Aminul Islam

List of Publications by Year
in descending order

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181 papers	1,974 citations	331259 21 h-index	344852 36 g-index
197 all docs	197 docs citations	197 times ranked	833 citing authors

#	Article	IF	Citations
1	Leakage Characterization of 10T SRAM Cell. IEEE Transactions on Electron Devices, 2012, 59, 631-638.	1.6	132
2	Variation Tolerant Differential 8T SRAM Cell for Ultralow Power Applications. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, 35, 549-558.	1.9	111
3	Advances in Ultrasonic Welding of Thermoplastic Composites: A Review. Materials, 2020, 13, 1284.	1.3	100
4	A technique to mitigate impact of process, voltage and temperature variations on design metrics of SRAM Cell. Microelectronics Reliability, 2012, 52, 405-411.	0.9	94
5	9-T SRAM Cell for Reliable Ultralow-Power Applications and Solving Multibit Soft-Error Issue. IEEE Transactions on Device and Materials Reliability, 2016, 16, 172-182.	1.5	74
6	Optimized Design of a 32-nm CNFET-Based Low-Power Ultrawideband CCII. IEEE Nanotechnology Magazine, 2012, 11, 1100-1109.	1.1	51
7	Characterization of Half-Select Free Write Assist 9T SRAM Cell. IEEE Transactions on Electron Devices, 2019, 66, 4745-4752.	1.6	47
8	Variability aware low leakage reliable SRAM cell design technique. Microelectronics Reliability, 2012, 52, 1247-1252.	0.9	45
9	Effect of potassium fertilization on yield and potassium nutrition of Boro rice in a wetland ecosystem of Bangladesh. Archives of Agronomy and Soil Science, 2016, 62, 1530-1540.	1.3	45
10	Half-Select-Free Low-Power Dynamic Loop-Cutting Write Assist SRAM Cell for Space Applications. IEEE Transactions on Electron Devices, 2020, 67, 80-89.	1.6	43
11	A highly stable reliable SRAM cell design for low power applications. Microelectronics Reliability, 2020, 105, 113503.	0.9	39
12	Design of Soft-Error-Aware SRAM With Multi-Node Upset Recovery for Aerospace Applications. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 2470-2480.	3.5	38
13	Transmission gateâ€based 9T SRAM cell for variation resilient low power and reliable internet of things applications. IET Circuits, Devices and Systems, 2019, 13, 584-595.	0.9	34
14	Floating active inductor based Class-C VCO with 8 digitally tuned sub-bands. AEU - International Journal of Electronics and Communications, 2018, 83, 1-10.	1.7	33
15	Design of Power- and Variability-Aware Nonvolatile RRAM Cell Using Memristor as a Memory Element. IEEE Journal of the Electron Devices Society, 2019, 7, 701-709.	1.2	33
16	A 2.5 GHz Low Power, High- ${Q}$, Reliable Design of Active Bandpass Filter. IEEE Transactions on Device and Materials Reliability, 2017, 17, 229-244.	1.5	32
17	Circuitâ€level design technique to mitigate impact of process, voltage and temperature variations in complementary metalâ€oxide semiconductor full adder cells. IET Circuits, Devices and Systems, 2015, 9, 204-212.	0.9	31
18	Soft-Error Resilient Read Decoupled SRAM With Multi-Node Upset Recovery for Space Applications. IEEE Transactions on Electron Devices, 2021, 68, 2246-2254.	1.6	31

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19	Variation resilient subthreshold SRAM cell design technique. International Journal of Electronics, 2012, 99, 1223-1237.	0.9	30
20	Optimization of SiC UMOSFET Structure for Improvement of Breakdown Voltage and ON-Resistance. IEEE Transactions on Electron Devices, 2018, 65, 615-621.	1.6	28
21	Characterization of AlGaN/GaN and AlGaN/AlN/GaN HEMTs in terms of mobility and subthreshold slope. Journal of Computational Electronics, 2016, 15, 172-180.	1.3	24
22	Highly Stable Low Power Radiation Hardened Memory-by-Design SRAM for Space Applications. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 2147-2151.	2.2	21
23	Design of 10T full adder cell for ultralow-power applications. Ain Shams Engineering Journal, 2018, 9, 2363-2372.	3.5	20
24	Effect of Process Parameters on Flow Length and Flash Formation in Injection Moulding of High Aspect Ratio Polymeric Micro Features. Micromachines, 2018, 9, 58.	1.4	20
25	Reliable write assist low power SRAM cell for wireless sensor network applications. IET Circuits, Devices and Systems, 2020, 14, 137-147.	0.9	19
26	Variability analysis and FinFET-based design of XOR and XNOR circuit. , 2011, , .		18
27	Direct electroplating of plastic for advanced electrical applications. CIRP Annals - Manufacturing Technology, 2017, 66, 209-212.	1.7	18
28	Soft-Error-Immune Read-Stability-Improved SRAM for Multi-Node Upset Tolerance in Space Applications. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 3317-3327.	3.5	18
29	VARIABILITY ANALYSIS OF 6T AND 7T SRAM CELL IN SUB-45NM TECHNOLOGY. IIUM Engineering Journal, 2011, 12, 13-30.	0.5	18
30	Reliable and Q -Enhanced Floating Active Inductors and Their Application in RF Bandpass Filters. IEEE Access, 2018, 6, 48181-48194.	2.6	17
31	A VDTA-based robust electronically tunable memristor emulator circuit. Analog Integrated Circuits and Signal Processing, 2020, 104, 47-59.	0.9	17
32	Quality investigation of miniaturized Moulded Interconnect Devices (MIDs) for hearing aid applications. CIRP Annals - Manufacturing Technology, 2015, 64, 539-544.	1.7	14
33	Design and development of memristorâ€based RRAM. IET Circuits, Devices and Systems, 2019, 13, 548-557.	0.9	14
34	Characterization of InP-based pseudomorphic HEMT with T-gate. Microsystem Technologies, 2020, 26, 2183-2191.	1.2	14
35	The Influence of the Hybridization Process on the Mechanical and Thermal Properties of Polyoxymethylene (POM) Composites with the Use of a Novel Sustainable Reinforcing System Based on Biocarbon and Basalt Fiber (BC/BF). Materials, 2020, 13, 3496.	1.3	14
36	Design of differential TG based 8T SRAM cell for ultralow-power applications. Microsystem Technologies, 2020, 26, 3299-3310.	1.2	13

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37	Design of low power, variation tolerant single bitline 9T SRAM cell in 16-nm technology in subthreshold region. Microelectronics Reliability, 2021, 120, 114126.	0.9	13
38	Soft-Error-Aware Read-Decoupled SRAM With Multi-Node Recovery for Aerospace Applications. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 3336-3340.	2.2	13
39	Nonvolatile and Robust Design of Content Addressable Memory Cell Using Magnetic Tunnel Junction at Nanoscale Regime. IEEE Transactions on Magnetics, 2015, 51, 1-13.	1.2	12
40	Variationâ€aware widely tunable nanoscale design of CMOS active inductorâ€based RF bandpass filter. International Journal of Circuit Theory and Applications, 2017, 45, 2181-2200.	1.3	12
41	Interaction of nanofillers in injection-molded graphene/carbon nanotube reinforced PA66 hybrid nanocomposites. Journal of Polymer Engineering, 2018, 38, 971-981.	0.6	12
42	Comparative study of CMOS- and FinFET-based 10T SRAM cell in subthreshold regime. , 2014, , .		11
43	Design of a Stable Read-Decoupled 6T SRAM Cell at 16-Nm Technology Node. , 2015, , .		11
44	Analytical Modeling of Wrap-Gate Carbon Nanotube FET With Parasitic Capacitances and Density of States. IEEE Transactions on Electron Devices, 2016, 63, 3314-3319.	1.6	11
45	Circuit-Level Technique to Design Variation- and Noise-Aware Reliable Dynamic Logic Gates. IEEE Transactions on Device and Materials Reliability, 2018, 18, 224-239.	1.5	11
46	Design of memristor based low power and highly reliable ReRAM cell. Microsystem Technologies, 2022, 28, 793-807.	1.2	11
47	Study of high Al fraction in AlGaN barrier HEMT and GaN and InGaN channel HEMT with In0.17Al0.83N barrier. Microsystem Technologies, 2020, 26, 2145-2158.	1.2	11
48	Radiationâ€hardened readâ€decoupled lowâ€power 12T SRAM for space applications. International Journal of Circuit Theory and Applications, 2021, 49, 3583-3596.	1.3	11
49	Energy Efficient and Process Tolerant Full Adder Design in Near Threshold Region Using FinFET. , 2010, , .		10
50	Design and Analysis of Robust Dual Threshold CMOS Full Adder Circuit in 32nm Technology. , 2010, , .		10
51	Implementation of FinFET based STT-MRAM bitcell. , 2014, , .		10
52	TG based 2T2M RRAM using Memristor as Memory Element. Indian Journal of Science and Technology, 2016, 9, .	0.5	10
53	A CMOS active inductor based digital and analog dual tuned voltage-controlled oscillator. Microsystem Technologies, 2019, 25, 1571-1583.	1.2	10
54	Characterization of <scp>AlGaN</scp>/<scp>GaN</scp> based <scp>HEMT</scp> for low noise and high frequency application. International Journal of Numerical Modelling: Electronic Networks, Devices and Fields, 2022, 35, e2932.	1.2	10

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55	Robust Design of CNFET Based Buffered Delay Model and Microwave Pulse Generator. , 2014, , .		9
56	Comparative analysis of D flip-flops in terms of delay and its variability. , 2015, , .		9
57	Characterization of AlGaN and GaN Based HEMT with AlN Interfacial Spacer. , 2015, , .		9
58	Technology scaling and its side effects. , 2015, , .		9
59	Power-aware sourse feedback single-ended 7T SRAM cell at nanoscale regime. Microsystem Technologies, 2019, 25, 1783-1791.	1.2	9
60	Design of resistive random access memory cell and its architecture. Microsystem Technologies, 2020, 26, 1325-1332.	1.2	9
61	Architecture of resistive RAM with write driver. Solid State Electronics Letters, 2020, 2, 10-22.	1.0	9
62	Robust subthreshold full adder design technique. , 2011, , .		8
63	Trigger Pulse Generator Using Proposed Buffered Delay Model and Its Application. Active and Passive Electronic Components, 2015, 2015, 1-9.	0.3	8
64	Gate Design in Injection Molding of Microfluidic Components Using Process Simulations. Journal of Micro and Nano-Manufacturing, 2016, 4, .	0.8	8
65	Design of CNFET based power- and variability-aware nonvolatile RRAM cell. Microelectronics Journal, 2019, 86, 7-14.	1.1	8
66	Comprehensive characterization and material modeling for ceramic injection molding simulation performance validations. International Journal of Advanced Manufacturing Technology, 2019, 102, 225-240.	1.5	8
67	Design of SRAM cell for low power portable healthcare applications. Microsystem Technologies, 2022, 28, 833-844.	1.2	8
68	Threshold voltage extraction and its reliance on device parameters @ 16-nm process technology. , 2015, , .		7
69	Device bias technique to improve design metrics of 6T SRAM cell for subthreshold operation. , 2015, , .		7
70	Comparative analysis of various 9T SRAM cell at 22-nm technology node. , 2015, , .		7
71	Correlation of mechanical and electrical properties with processing variables in MWCNT reinforced thermoplastic nanocomposites. Journal of Composite Materials, 2018, 52, 3681-3697.	1.2	7
72	Variation resilient low-power memristor-based synchronous flip-flops: design and analysis. Microsystem Technologies, 2021, 27, 525-538.	1.2	7

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73	Power - and variability-aware design of FinFET-based XOR circuit at nanoscale regime. , 2014, , .		6
74	Optimized design of Au-polysilicon electrothermal microgripper for handling micro objects. , 2015, , .		6
75	A Compact Low Power High Frequency Pulse Generator. , 2015, , .		6
76	Comparative study of subthreshold leakage in CNFET & MOSFET @ 32-nm technology node. , 2016, , .		6
77	Design of magnetic tunnel junctionâ€based tunable spin torque oscillator at nanoscale regime. IET Circuits, Devices and Systems, 2016, 10, 121-129.	0.9	6
78	Low-power half-select free single-ended 10 transistor SRAM cell. Microsystem Technologies, 2017, 23, 4133-4144.	1.2	6
79	Analysis of AlGaN/GaN high electron mobility transistor for high frequency application. , 2017, , .		6
80	Comparative analysis of AlGaN/GaN high electron mobility transistor with sapphire and 4H-SiC substrate. Microsystem Technologies, 2019, 25, 1927-1935.	1.2	6
81	Characterization of single-ended 9T SRAM cell. Microsystem Technologies, 2020, 26, 1591-1604.	1.2	6
82	Study and Analysis of AlInN/GaN Based High Electron Mobility Transistor. Lecture Notes in Electrical Engineering, 2020, , 449-459.	0.3	6
83	Variability Immune FinFET-Based Full Adder Design in Subthreshold Region. , 2011, , .		5
84	Experimental investigation of new manufacturing process chains to create micro-metal structures on polymer substrates for lab-on-chip sensors. International Journal of Advanced Manufacturing Technology, 2012, 59, 101-109.	1.5	5
85	CNFET Based Voltage Multiplier Circuit for RF Energy Harvesting Applications. , 2015, , .		5
86	Analysis of breakdown voltage of a field plated High Electron Mobility Transistor. , 2017, , .		5
87	Design and analysis of MISO bi-quad active filter. International Journal of Electronics, 2019, 106, 287-304.	0.9	5
88	An Analysis and Modeling of the Class-E Inverter for ZVS/ZVDS at Any Duty Ratio with High Input Ripple Current. Electronics (Switzerland), 2021, 10, 1312.	1.8	5
89	Effect of Source, Drain and Channel Spacing from Gate of HEMT. Lecture Notes in Electrical Engineering, 2020, , 81-90.	0.3	5
90	Al_{0.30}Ga_{0.70}N /GaN MODFET with triple-teeth metal for RF and high-power applications. Physica Scripta, 2022, 97, 034003.	1.2	5

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91	Variability Analysis of MTJ-Based Circuit. , 2012, , .		4
92	Investigation of robust full adder cell in 16-nm CMOS technology node. , 2013, , .		4
93	CNFET-based ternary inverter and its variability analysis. , 2014, , .		4
94	CNFET-based 0.1 V to 0.6 V DC/DC converter. , 2014, , .		4
95	Low-power 9T subthreshold SRAM cell with single-ended write scheme. , 2015, , .		4
96	CNFET-Based 0.1- to 1.2-V DC/DC Boost Converter With Voltage Regulation for Energy Harvesting Applications. IEEE Nanotechnology Magazine, 2015, 14, 660-667.	1.1	4
97	Which is the Best 2-to-1 Line Multiplexer for Ultralow-Power Applications?. , 2015, , .		4
98	Low Power and High Variation Tolerant 9T-SRAM Cell at 16-nm Technology Node. Indian Journal of Science and Technology, 2016, 9, .	0.5	4
99	Characterisation of field plated high electron mobility transistor. , 2016, , .		4
100	Current-mode circuit-level technique to design variation-aware nanoscale summing circuit for ultra-low power applications. Microsystem Technologies, 2017, 23, 4045-4056.	1.2	4
101	Study of variability performance of CMOS active inductors. Microsystem Technologies, 2020, 26, 3101-3111.	1.2	4
102	A novel CNFET based tunable memristor emulator. Microsystem Technologies, 2020, 26, 2173-2181.	1.2	4
103	A low power SRAM cell design for wireless sensor network applications. Microsystem Technologies, 2020, 26, 2325-2335.	1.2	4
104	Radiation-Hardened Low Read Delay 12T-SRAM Cell for Space Applications. , 2021, , .		4
105	AlGaN/GaN HEMT with Recessed T-Gate and Floating Metal for High Power Applications. , 2021, , .		4
106	A Monotonic Digitally Controlled Delay Element-Based Programmable Trigger Pulse Generator. Advances in Intelligent Systems and Computing, 2016, , 365-374.	0.5	4
107	Design of variation-resilient CNFET-based Schmitt trigger circuits with optimum hysteresis at 16-nm technology node. , 2013, , .		3
108	Highly stable subthreshold single-ended 7T SRAM cell. , 2014, , .		3

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109	Power and variability analysis of CMOS logic families @ 22-nm technology node. , 2014, , .		3
110	Stability and variability enhancement of 9T SRAM cell for subthreshold operation. , 2014, , .		3
111	Revisiting performance of various delay elements to realize a trigger pulse generator. , 2015, , .		3
112	7-Transistor 2-memristor based non-volatile static random access memory cell design. , 2015, , .		3
113	MOSFET aspect ratio optimization for minimized transistor mismatch at UDSM technology nodes. , 2015, , .		3
114	Design of hybrid full adder in deep subthreshold region for ultralow power applications. , 2015, , .		3
115	Validation of precision powder injection molding process simulations using a spiral test geometry. AIP Conference Proceedings, 2016, , .	0.3	3
116	Multi-gate device and summing-circuit co-design robustness studies @ 32-nm technology node. Microsystem Technologies, 2017, 23, 4099-4109.	1.2	3
117	Analysis of various delay elements @ 16-nm technology node. , 2017, , .		3
118	Compact design of an MTJ-based non-volatile CAM cell with read/write operations. Microsystem Technologies, 2020, 26, 3259-3270.	1.2	3
119	A Highly Reliable and Radiation-Hardened Majority PFET-Based 10T SRAM Cell. Lecture Notes in Electrical Engineering, 2021, , 113-122.	0.3	3
120	Design and Analysis of Robust Spin Transfer Torque Magnetic Random Access Memory Bitcell Using FinFET. Journal of Low Power Electronics, 2014, 10, 220-227.	0.6	3
121	Performance optimization of LUT of subthreshold FPGA in deep submicron. , 2010, , .		2
122	Optimized design of hybrid CMOS and CNFET 32 nm dual-X current conveyor. , 2011, , .		2
123	Power optimized variation aware dual-threshold SRAM cell design technique. Nanotechnology, Science and Applications, 2011, 4, 25.	4.6	2
124	FinFET-based variation resilient 8T SRAM cell. , 2012, , .		2
125	Performance evaluation of CNFET based operational amplifier at technology node beyond 45-nm. , 2013, , .		2
126	Performance evaluation of MCML-based XOR/XNOR circuit at 16-nm Technology node. , 2014, , .		2

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127	Robustness study and CNFET realization of optimal logic circuit for ultralow power applications. , 2014, , .		2
128	CMOS based compact wide band tunable active inductor design. , 2015, , .		2
129	Experimental Investigation of Comparative Process Capabilities of Metal and Ceramic Injection Molding for Precision Applications. Journal of Micro and Nano-Manufacturing, 2016, 4, .	0.8	2
130	Development of data acquisition system and data analysis technique for automotive applications. , 2016, , .		2
131	Investigation on electrical characteristics of FDSOI device for ultra-low power operation. , 2016, , .		2
132	A comparative analysis of various programmable delay elements using predictive technology model. , 2016, , .		2
133	A double trench 4H â€" SiC MOSFET as an enhanced model of SiC UMOSFET. , 2017, , .		2
134	Analysis of Al<inf>0.22</inf>Ga<inf>0.78</inf>As/In<inf>0.18</inf>Ga<inf>0.82</inf>As/GaAs2 Pseudomorphic HEMT device with higher conductivity. , 2017, , .		
135	Performance comparison of AlGaN/GaN HFET with sapphire and 4H-SiC substrate. , 2017, , .		2
136	Development of HEMT device with surface passivation for a low leakage current and steep subthreshold slope. , 2017, , .		2
137	An efficient circuit-level power reduction technique for ultralow power applications. Microsystem Technologies, 2019, 25, 1689-1697.	1.2	2
138	Blister Formation in Film Insert Moulding. Micromachines, 2020, 11, 424.	1.4	2
139	A Comparative Performance Analysis of Zero Voltage Switching Class E and Selected Enhanced Class E Inverters. Electronics (Switzerland), 2021, 10, 2226.	1.8	2
140	A Current-Mode Memristor Emulator Circuit. Lecture Notes in Electrical Engineering, 2020, , 493-501.	0.3	2
141	Power and variability aware design of SRAM using carbon nanotube field effect transistor. , 2010, , .		1
142	Design of 2∶1 multiplexer and 1∶2 demultiplexer using magnetic tunnel junction elements. , 2013, , .		1
143	Design metrics improvement of 10TSRAM cell using CNFET. , 2014, , .		1
144	Characterization of Phase-Change Material Using Verilog-A and its Validation as a Memory Element. , 2014, , .		1

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145	Design of CNFET based charge pump for RF energy harvesting applications. , 2015, , .		1
146	An ultralow-power low-voltage Class-AB Fully Differential Op Amp with cascoded input stage and indirect compensation. , 2015, , .		1
147	Low Voltage Charge Pump for RF Energy Harvesting Applications. Indian Journal of Science and Technology, 2016, 9, .	0.5	1
148	Design of 10T SRAM Cell using Column-Line Assist and DTMOS Techniques. Indian Journal of Science and Technology, 2016, 9, .	0.5	1
149	Investigating Phase Transform Behavior in Indium Selenide Based RAM and Its Validation as a Memory Element. Journal of Materials, 2016, 2016, 1-7.	0.1	1
150	High breakdown (958 V) low threshold GaN HEMT. , 2017, , .		1
151	Compact Versatile Noise Suppressed Programmable Trigger Pulse Generator for Industrial Applications. The National Academy of Sciences, India, 2018, 41, 97-101.	0.8	1
152	Performance Enhancement of Full Adder Circuit: Current Mode Operated Majority Function Based Design. Advances in Intelligent Systems and Computing, 2018, , 569-578.	0.5	1
153	Process chains for the mass production of transparent crowns for posterior teeth. CIRP Annals - Manufacturing Technology, 2019, 68, 591-594.	1.7	1
154	A low power, temperature compensated, robust design of CS amplifier in nanoscale regime. Microsystem Technologies, 2019, 25, 1841-1852.	1.2	1
155	Enhanced Energy Savings in Indoor Environments with Effective Daylight Utilization and Area Segregation. Symmetry, 2020, 12, 1313.	1.1	1
156	Robust Design of Noise Tolerant 2-Phase Non Overlapping Clock Generating Circuit. , 2021, , .		1
157	High Speed Cache Design Using Multi-diameter CNFET at 32nm Technology. Communications in Computer and Information Science, 2010, , 215-222.	0.4	1
158	A Technique for Designing Variation Resilient Subthreshold Sram Cell. IIUM Engineering Journal, 2013, 14, .	0.5	1
159	Variation resilient reliable design of trigger pulse generator. IET Circuits, Devices and Systems, 2020, 14, 860-868.	0.9	1
160	Design and Development of Clocked Transmission Gate Cross-Coupled Adiabatic Circuit. , 2009, , .		0
161	Low Active Power High Speed Cache Design. , 2011, , .		0
162	Variation mitigation technique in SRAM cell using adaptive body bias. , 2012, , .		0

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163	Threshold voltage extraction techniques for device @ 16 nm technology node. , 2015, , .		0
164	Propagation delay and its robustness study of inverter topologies. , 2015, , .		0
165	Performance improvement in 4H-SiC UMOSFET with HfO<inf>2</inf>/Al<inf>2</inf>O<inf>3</inf> gate dielectric stack. , 2017, , .		0
166	Compact 6T design of voltage controlled tunable resistor for high frequency applications. , 2017, , .		0
167	Study of Al<inf>0.22</inf>Ga<inf>0.78</inf>As/In<inf>0.18</inf>Ga<inf>0.82</inf>As/GaAs PHEMT with delta doping and lower Al mole fraction. , 2017, , .		0
168	An Electronically-Tuneable VDTA Based Sinusoidal Oscillator. Communications in Computer and Information Science, 2018, , 115-123.	0.4	0
169	Optimization of InP HEMT Using Multilayered Cap and Asymmetric Gate Recess. Communications in Computer and Information Science, 2018, , 19-28.	0.4	0
170	Multi-functional Active Filter Design Using Three VDTAs. Communications in Computer and Information Science, 2018, , 124-130.	0.4	0
171	Modeling and sizing of non-linear CMOS analog circuits used in mixed signal systems. Analog Integrated Circuits and Signal Processing, 2019, 99, 95-109.	0.9	0
172	Design of a Signal Sensor for Analyzing Biological Activities at Cellular Level. Advances in Intelligent Systems and Computing, 2015, , 405-412.	0.5	0
173	Low-Leakage, Low-Power, High-Stable SRAM Cell Design. Advances in Intelligent Systems and Computing, 2016, , 549-556.	0.5	0
174	Design of a Low-Delay-Write Model of a TMCAM. Advances in Intelligent Systems and Computing, 2016, , 41-47.	0.5	0
175	Study and Analysis of Subthreshold Leakage Current in Sub-65Ânm NMOSFET. Advances in Intelligent Systems and Computing, 2016, , 1-10.	0.5	0
176	Estimation of MOS Capacitance Across Different Technology Nodes. Advances in Intelligent Systems and Computing, 2017, , 297-306.	0.5	0
177	Cross-Coupled Dynamic CMOS Latches: Robustness Study of Timing. Advances in Intelligent Systems and Computing, 2017, , 317-325.	0.5	0
178	Active Multifunctional Filter Design Using Carbon Nanotube Transistors. Lecture Notes in Electrical Engineering, 2020, , 103-111.	0.3	0
179	A Fully Integrated Tunable Memristor Emulator Circuit. Lecture Notes in Electrical Engineering, 2020, , 553-560.	0.3	0
180	A Technique to Design Robust Single-Stage Operational Amplifier. Lecture Notes in Electrical Engineering, 2020, , 469-478.	0.3	0

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181	Effects of Miniaturization on the Quality of Metallized Plastic Parts. Micromachines, 2022, 13, 515.	1.4	0