Koen Om De Bosschere

List of Publications by Year
in descending order

115	2,047	430442	360668
papers	citations	18 h-index	35 g-index

119	119	119	1112
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Adaptive Compiler Strategies for Mitigating Timing Side Channel Attacks. IEEE Transactions on Dependable and Secure Computing, 2020, 17, 35-49.	3.7	13
2	Effective and efficient Javaâ€type obfuscation. Software - Practice and Experience, 2020, 50, 136-160.	2.5	2
3	HiPEAC. Communications of the ACM, 2019, 62, 42-42.	3.3	0
4	Software-Directed Techniques for Improved GPU Register File Utilization. Transactions on Architecture and Code Optimization, 2018, 15, 1-23.	1.6	5
5	SOFIA: Software and control flow integrity architecture. Computers and Security, 2017, 68, 16-35.	4.0	30
6	Calling hardware procedures in a reconfigurable accelerator using RPC-FPGA. , 2017, , .		3
7	Evaluation of dynamic binary translation techniques for full system virtualisation on ARMv7-A. Journal of Systems Architecture, 2016, 65, 30-45.	2.5	4
8	Link-time smart card code hardening. International Journal of Information Security, 2016, 15, 111-130.	2.3	10
9	SOFIA: Software and Control Flow Integrity Architecture. , 2016, , .		28
10	Pushing Java Type Obfuscation to the Limit. IEEE Transactions on Dependable and Secure Computing, 2014, 11, 553-567.	3.7	6
11	Formal virtualization requirements for the ARM architecture. Journal of Systems Architecture, 2013, 59, 144-154.	2.5	10
12	Protecting Your Software Updates. IEEE Security and Privacy, 2013, 11, 47-54.	1.5	18
13	Mitigating Smart Card Fault Injection with Link-Time Code Rewriting: A Feasibility Study. Lecture Notes in Computer Science, 2013, , 221-229.	1.0	4
14	Introduction to the special issue on high-performance and embedded architectures and compilers. Transactions on Architecture and Code Optimization, 2012, 8, 1-2.	1.6	2
15	A profile-based tool for finding pipeline parallelism in sequential programs. Parallel Computing, 2010, 36, 531-551.	1.3	32
16	Implicit hints: Embedding hint bits in programs without ISA changes. , 2010, , .		2
17	Accelerating Multiple Sequence Alignment with the Cell BE Processor. Computer Journal, 2010, 53, 814-826.	1.5	5
18	The Paralax infrastructure. , 2010, , .		65

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19	Compilation and virtualization in the HiPEAC vision. , 2010, , .		5
20	Practical Mitigations for Timing-Based Side-Channel Attacks on Modern x86 Processors. , 2009, , .		133
21	Towards automatic program partitioning. , 2009, , .		6
22	System-scenario-based design of dynamic embedded systems. ACM Transactions on Design Automation of Electronic Systems, 2009, 14, 1-45.	1.9	122
23	Linux Kernel Compaction through Cold Code Swapping. Lecture Notes in Computer Science, 2009, , 173-200.	1.0	0
24	Upcoming Computing System Challenges â€“ The HiPEAC Vision Anstehende Herausforderungen der Computer Industrie â€“ Die HiPEAC Vision. IT - Information Technology, 2008, 50, 285-292.	0.6	0
25	Extracting coarse-grain parallelism in general-purpose programs. , 2008, , .		9
26	Constructing Optimal XOR-Functions to Minimize Cache Conflict Misses. Lecture Notes in Computer Science, 2008, , 261-272.	1.0	3
27	Towards Tamper Resistant Code Encryption: Practice and Experience. Lecture Notes in Computer Science, 2008, , 86-100.	1.0	22
28	Experiences with Parallelizing a Bio-informatics Program on the Cell BE. Lecture Notes in Computer Science, 2008, , 161-175.	1.0	6
29	Link-time compaction and optimization of ARM executables. Transactions on Embedded Computing Systems, 2007, 6, 5.	2.1	22
30	Automated reduction of the memory footprint of the Linux kernel. Transactions on Embedded Computing Systems, 2007, 6, 23.	2.1	15
31	Java object header elimination for reduced memory consumption in 64-bit virtual machines. Transactions on Architecture and Code Optimization, 2007, 4, 17.	1.6	7
32	Using hpm-sampling to drive dynamic compilation. ACM SIGPLAN Notices, 2007, 42, 553-568.	0.2	2
33	Program obfuscation. , 2007, , .		60
34	A practical interprocedural dominance algorithm. ACM Transactions on Programming Languages and Systems, 2007, 29, 19.	1.7	9
35	Function level parallelism driven by data dependencies. Computer Architecture News, 2007, 35, 55-62.	2.5	28
36	Exploiting program phase behavior for energy reduction on multi-configuration processors. Journal of Systems Architecture, 2007, 53, 489-500.	2.5	8

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37	Clustered indexing for branch predictors. Microprocessors and Microsystems, 2007, 31, 168-177.	1.8	1
38	High-Performance Embedded Architecture and Compilation Roadmap. Lecture Notes in Computer Science, 2007, , 5-29.	1.0	26
39	GCH: Hints for Triggering Garbage Collections. Lecture Notes in Computer Science, 2007, , 74-94.	1.0	5
40	A Model for Self-Modifying Code. Lecture Notes in Computer Science, 2007, , 232-248.	1.0	14
41	Run-Time Randomization to Mitigate Tampering. Lecture Notes in Computer Science, 2007, , 153-168.	1.0	6
42	Using hpm-sampling to drive dynamic compilation. , 2007, , .		18
43	Object-Relative Addressing: Compressed Pointers in 64-Bit Java Virtual Machines. Lecture Notes in Computer Science, 2007, , 79-100.	1.0	2
44	Software Protection Through Dynamic Code Mutation. Lecture Notes in Computer Science, 2006, , 194-206.	1.0	45
45	64-bit versus 32-bit Virtual Machines for Java. Software - Practice and Experience, 2006, 36, 1-26.	2.5	4
46	On the expressiveness of timed coordination models. Science of Computer Programming, 2006, 61, 152-187.	1.5	13
47	Improved composite confidence mechanisms for a perceptron branch predictor. Journal of Systems Architecture, 2006, 52, 143-151.	2.5	0
48	Bidirectional liveness analysis, or how less than half of the Alphaâ€™s registers are used. Journal of Systems Architecture, 2006, 52, 535-548.	2.5	3
49	Yet shorter warmup by combining no-state-loss and MRRL for sampled LRU cache simulation. Journal of Systems and Software, 2006, 79, 645-652.	3.3	5
50	An Analysis of Program Phase Behavior and its Predictability. AIP Conference Proceedings, 2006, , .	0.3	1
51	Javana. ACM SIGPLAN Notices, 2006, 41, 153-168.	0.2	8
52	Exploiting Video Stream Similarity for Energy-Efficient Decoding. Lecture Notes in Computer Science, 2006, , 11-22.	1.0	6
53	System-wide compaction and specialization of the linux kernel. ACM SIGPLAN Notices, 2005, 40, 95-104.	0.2	2
54	Optimal sample length for efficient cache simulation. Journal of Systems Architecture, 2005, 51, 513-525.	2.5	1

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55	Offline Phase Analysis and Optimization for Multi-configuration Processors. Lecture Notes in Computer Science, 2005, , 202-211.	1.0	4
56	Link-time binary rewriting techniques for program compaction. ACM Transactions on Programming Languages and Systems, 2005, 27, 882-945.	1.7	49
57	BLRL: Accurate and Efficient Warmup for Sampled Processor Simulation. Computer Journal, 2005, 48, 451-459.	1.5	36
58	Steganography for Executables and Code Transformation Signatures. Lecture Notes in Computer Science, 2005, , 425-439.	1.0	20
59	A Detailed Study on Phase Predictors. Lecture Notes in Computer Science, 2005, , 571-581.	1.0	12
60	Using Decision Trees to Improve Program-Based and Profile-Based Static Branch Prediction. Lecture Notes in Computer Science, 2005, , 336-352.	1.0	4
61	Comparing Low-Level Behavior of SPEC CPU and Java Workloads. Lecture Notes in Computer Science, 2005, , 669-679.	1.0	3
62	Garbage Collection Hints. Lecture Notes in Computer Science, 2005, , 233-248.	1.0	8
63	Method-level phase behavior in java workloads. , 2004, , .		49
64	Evaluation of the Gini-index for Studying Branch Prediction Features. AIP Conference Proceedings, 2004, , .	0.3	1
65	The design and implementation of FIT. , 2004, , .		20
66	Speeding Up Architectural Simulations for High-Performance Processors. Simulation, 2004, 80, 451-468.	1.1	4
67	Towards an Extensible Context Ontology for Ambient Intelligence. Lecture Notes in Computer Science, 2004, , 148-159.	1.0	195
68	Efficient Architectural Design of High Performance Microprocessors. Advances in Computers, 2004, 61, 45-106.	1.2	0
69	On Generating Set Index Functions for Randomized Caches. Computer Journal, 2004, 47, 245-258.	1.5	1
70	Control Flow Modeling in Statistical Simulation for Accurate and Efficient Processor Design Studies. Computer Architecture News, 2004, 32, 350.	2.5	44
71	Method-level phase behavior in java workloads. ACM SIGPLAN Notices, 2004, 39, 270-287.	0.2	6
72	How accurate should early design stage power/performance tools be? A case study with statistical simulation. Journal of Systems and Software, 2004, 73, 45-62.	3.3	1

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73	Efficient simulation of trace samples on parallel machines. Parallel Computing, 2004, 30, 317-335.	1.3	8
74	Low-level behavioral analysis of the JVT/AVC decoder. , 2004, 5308, 1371.		0
75	Detecting Data Races in Sequential Programs with DIOTA. Lecture Notes in Computer Science, 2004, , 82-89.	1.0	7
76	Link-Time Optimization of IA64 Binaries. Lecture Notes in Computer Science, 2004, , 284-291.	1.0	7
77	Link-time optimization of ARM binaries. , 2004, , .		32
78	Link-time optimization of ARM binaries. ACM SIGPLAN Notices, 2004, 39, 211-220.	0.2	11
79	Debugging shared memory parallel programs using record/replay. Future Generation Computer Systems, 2003, 19, 679-687.	4.9	7
80	Quantifying behavioral differences between multimedia and general-purpose workloads. Journal of Systems Architecture, 2003, 48, 199-220.	2.5	1
81	Highly accurate and efficient evaluation of randomising set index functions. Journal of Systems Architecture, 2003, 48, 429-452.	2.5	3
82	On the side-effects of code abstraction. ACM SIGPLAN Notices, 2003, 38, 244-253.	0.2	3
83	How java programs interact with virtual machines at the microarchitectural level. ACM SIGPLAN Notices, 2003, 38, 169-186.	0.2	10
84	How java programs interact with virtual machines at the microarchitectural level. , 2003, , .		58
85	Record/replay for nondeterministic program executions. Communications of the ACM, 2003, 46, 62-67.	3.3	48
86	Bounding the number of segment histories during data race detection. Parallel Computing, 2002, 28, 1221-1238.	1.3	2
87	Non-Intrusive Detection of Synchronization Errors Using Execution Replay. Automated Software Engineering, 2002, 9, 95-121.	2.2	7
88	Sifting out the mud. , 2002, , .		24
89	Sifting out the mud. ACM SIGPLAN Notices, 2002, 37, 275-291.	0.2	3
90	Independent Hashing as Confidence Mechanism for Value Predictors in Microprocessors. Lecture Notes in Computer Science, 2002, , 458-467.	1.0	0

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91	A Comparative Study of Redundancy in Trace Caches. Lecture Notes in Computer Science, 2002, , 512-516.	1.0	1
92	Nonuniform behavior in instruction traces for contemporary processors. AIP Conference Proceedings, 2001, , .	0.3	0
93	Combining Global Code and Data Compaction. ACM SIGPLAN Notices, 2001, 36, 29-38.	0.2	3
94	Blackboard relations in the Î¼Log coordination model. New Generation Computing, 2001, 19, 23-55.	2.5	5
95	alto: a linkâ€time optimizer for the Compaq Alpha. Software - Practice and Experience, 2001, 31, 67-101.	2.5	54
96	Combining Global Code and Data Compaction. , 2001, , .		15
97	alto: a link-time optimizer for the Compaq Alpha. , 2001, 31, 67.		32
98	TRaDe: Data Race Detection for Java. Lecture Notes in Computer Science, 2001, , 761-770.	1.0	10
99	JiTI. Computer Architecture News, 2001, 29, 43-54.	2.5	4
100	Early design stage exploration of fixed-length block structured architectures. Journal of Systems Architecture, 2000, 46, 1469-1486.	2.5	1
101	ESTIMATING IPC OF A BLOCK STRUCTURED INSTRUCTION SET ARCHITECTURE IN AN EARLY DESIGN STAGE. , 2000, , .		3
102	A Comparison of Locality-Based and Recency-Based Replacement Policies. Lecture Notes in Computer Science, 2000, , 310-318.	1.0	0
103	INCREASING THE EFFICIENCY OF VALUE PREDICTION IN FUTURE PROCESSORS BY PREDICTING LESS. , 2000, , .		0
104	RecPlay. ACM Transactions on Computer Systems, 1999, 17, 133-152.	0.6	241
105	Exploitable levels of ILP in future processors. Journal of Systems Architecture, 1999, 45, 687-708.	2.5	5
106	A fast, cache-aware algorithm for the calculation of radiological paths exploiting subword parallelism. Journal of Systems Architecture, 1999, 45, 781-790.	2.5	26
107	LogiMOO: An extensible multi-user virtual world with natural language control. The Journal of Logic Programming, 1999, 38, 331-353.	1.9	15
108	On the use of subword parallelism in medical image processing. Parallel Computing, 1998, 24, 1537-1556.	1.3	4

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109	TARILAN: an embedded functional data processing language. Journal of Systems and Software, 1998, 43, 93-102.	3.3	2
110	JiTI: Tracing Memory References for Data Race Detection. Advances in Parallel Computing, 1998, 12, 327-334.	0.3	2
111	On Delphi lemmas and other memoing techniques for deterministic logic programs. The Journal of Logic Programming, 1997, 30, 145-163.	1.9	2
112	Process-based parallel logic programming: A survey of the basic issues. Journal of Systems and Software, 1997, 39, 71-82.	3.3	4
113	An Operator Precedence Parser for Standard Prolog Text. Software - Practice and Experience, 1996, 26, 763-779.	2.5	8
114	Extending the Î¼Log Framework with Local and Conditional Blackboard Operations. Journal of Symbolic Computation, 1996, 21, 669-697.	0.5	4
115	Partial translation: towards a portable and efficient prolog implementation technology. The Journal of Logic Programming, 1996, 29, 65-83.	1.9	10