Koen Om De Bosschere

List of Publications by Year
in descending order

115	2,047	430442	360668
papers	citations	18 h-index	35 g-index

119	119	119	1112
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	RecPlay. ACM Transactions on Computer Systems, 1999, 17, 133-152.	0.6	241
2	Towards an Extensible Context Ontology for Ambient Intelligence. Lecture Notes in Computer Science, 2004, , 148-159.	1.0	195
3	Practical Mitigations for Timing-Based Side-Channel Attacks on Modern x86 Processors. , 2009, , .		133
4	System-scenario-based design of dynamic embedded systems. ACM Transactions on Design Automation of Electronic Systems, 2009, 14, 1-45.	1.9	122
5	The Paralax infrastructure. , 2010, , .		65
6	Program obfuscation. , 2007, , .		60
7	How java programs interact with virtual machines at the microarchitectural level. , 2003, , .		58
8	alto: a linkâ€time optimizer for the Compaq Alpha. Software - Practice and Experience, 2001, 31, 67-101.	2.5	54
9	Method-level phase behavior in java workloads. , 2004, , .		49
10	Link-time binary rewriting techniques for program compaction. ACM Transactions on Programming Languages and Systems, 2005, 27, 882-945.	1.7	49
11	Record/replay for nondeterministic program executions. Communications of the ACM, 2003, 46, 62-67.	3.3	48
12	Software Protection Through Dynamic Code Mutation. Lecture Notes in Computer Science, 2006, , 194-206.	1.0	45
13	Control Flow Modeling in Statistical Simulation for Accurate and Efficient Processor Design Studies. Computer Architecture News, 2004, 32, 350.	2.5	44
14	BLRL: Accurate and Efficient Warmup for Sampled Processor Simulation. Computer Journal, 2005, 48, 451-459.	1.5	36
15	A profile-based tool for finding pipeline parallelism in sequential programs. Parallel Computing, 2010, 36, 531-551.	1.3	32
16	alto: a link-time optimizer for the Compaq Alpha. , 2001, 31, 67.		32
17	Link-time optimization of ARM binaries. , 2004, , .		32
18	SOFIA: Software and control flow integrity architecture. Computers and Security, 2017, 68, 16-35.	4.0	30

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19	Function level parallelism driven by data dependencies. Computer Architecture News, 2007, 35, 55-62.	2.5	28
20	SOFIA: Software and Control Flow Integrity Architecture. , 2016, , .		28
21	A fast, cache-aware algorithm for the calculation of radiological paths exploiting subword parallelism. Journal of Systems Architecture, 1999, 45, 781-790.	2.5	26
22	High-Performance Embedded Architecture and Compilation Roadmap. Lecture Notes in Computer Science, 2007, , 5-29.	1.0	26
23	Sifting out the mud. , 2002, , .		24
24	Link-time compaction and optimization of ARM executables. Transactions on Embedded Computing Systems, 2007, 6, 5.	2.1	22
25	Towards Tamper Resistant Code Encryption: Practice and Experience. Lecture Notes in Computer Science, 2008, , 86-100.	1.0	22
26	The design and implementation of FIT. , 2004, , .		20
27	Steganography for Executables and Code Transformation Signatures. Lecture Notes in Computer Science, 2005, , 425-439.	1.0	20
28	Protecting Your Software Updates. IEEE Security and Privacy, 2013, 11, 47-54.	1.5	18
29	Using hpm-sampling to drive dynamic compilation. , 2007, , .		18
30	LogiMOO: An extensible multi-user virtual world with natural language control. The Journal of Logic Programming, 1999, 38, 331-353.	1.9	15
31	Combining Global Code and Data Compaction. , 2001, , .		15
32	Automated reduction of the memory footprint of the Linux kernel. Transactions on Embedded Computing Systems, 2007, 6, 23.	2.1	15
33	A Model for Self-Modifying Code. Lecture Notes in Computer Science, 2007, , 232-248.	1.0	14
34	On the expressiveness of timed coordination models. Science of Computer Programming, 2006, 61, 152-187.	1.5	13
35	Adaptive Compiler Strategies for Mitigating Timing Side Channel Attacks. IEEE Transactions on Dependable and Secure Computing, 2020, 17, 35-49.	3.7	13
36	A Detailed Study on Phase Predictors. Lecture Notes in Computer Science, 2005, , 571-581.	1.0	12

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37	Link-time optimization of ARM binaries. ACM SIGPLAN Notices, 2004, 39, 211-220.	0.2	11
38	Partial translation: towards a portable and efficient prolog implementation technology. The Journal of Logic Programming, 1996, 29, 65-83.	1.9	10
39	How java programs interact with virtual machines at the microarchitectural level. ACM SIGPLAN Notices, 2003, 38, 169-186.	0.2	10
40	Formal virtualization requirements for the ARM architecture. Journal of Systems Architecture, 2013, 59, 144-154.	2.5	10
41	Link-time smart card code hardening. International Journal of Information Security, 2016, 15, 111-130.	2.3	10
42	TRaDe: Data Race Detection for Java. Lecture Notes in Computer Science, 2001, , 761-770.	1.0	10
43	A practical interprocedural dominance algorithm. ACM Transactions on Programming Languages and Systems, 2007, 29, 19.	1.7	9
44	Extracting coarse-grain parallelism in general-purpose programs. , 2008, , .		9
45	An Operator Precedence Parser for Standard Prolog Text. Software - Practice and Experience, 1996, 26, 763-779.	2.5	8
46	Efficient simulation of trace samples on parallel machines. Parallel Computing, 2004, 30, 317-335.	1.3	8
47	Javana. ACM SIGPLAN Notices, 2006, 41, 153-168.	0.2	8
48	Exploiting program phase behavior for energy reduction on multi-configuration processors. Journal of Systems Architecture, 2007, 53, 489-500.	2.5	8
49	Garbage Collection Hints. Lecture Notes in Computer Science, 2005, , 233-248.	1.0	8
50	Non-Intrusive Detection of Synchronization Errors Using Execution Replay. Automated Software Engineering, 2002, 9, 95-121.	2.2	7
51	Debugging shared memory parallel programs using record/replay. Future Generation Computer Systems, 2003, 19, 679-687.	4.9	7
52	Java object header elimination for reduced memory consumption in 64-bit virtual machines. Transactions on Architecture and Code Optimization, 2007, 4, 17.	1.6	7
53	Detecting Data Races in Sequential Programs with DIOTA. Lecture Notes in Computer Science, 2004, , 82-89.	1.0	7
54	Link-Time Optimization of IA64 Binaries. Lecture Notes in Computer Science, 2004, , 284-291.	1.0	7

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55	Method-level phase behavior in java workloads. ACM SIGPLAN Notices, 2004, 39, 270-287.	0.2	6
56	Towards automatic program partitioning. , 2009, , .		6
57	Pushing Java Type Obfuscation to the Limit. IEEE Transactions on Dependable and Secure Computing, 2014, 11, 553-567.	3.7	6
58	Exploiting Video Stream Similarity for Energy-Efficient Decoding. Lecture Notes in Computer Science, 2006, , 11-22.	1.0	6
59	Run-Time Randomization to Mitigate Tampering. Lecture Notes in Computer Science, 2007, , 153-168.	1.0	6
60	Experiences with Parallelizing a Bio-informatics Program on the Cell BE. Lecture Notes in Computer Science, 2008, , 161-175.	1.0	6
61	Exploitable levels of ILP in future processors. Journal of Systems Architecture, 1999, 45, 687-708.	2.5	5
62	Blackboard relations in the Î¼Log coordination model. New Generation Computing, 2001, 19, 23-55.	2.5	5
63	Yet shorter warmup by combining no-state-loss and MRRL for sampled LRU cache simulation. Journal of Systems and Software, 2006, 79, 645-652.	3.3	5
64	Accelerating Multiple Sequence Alignment with the Cell BE Processor. Computer Journal, 2010, 53, 814-826.	1.5	5
65	Software-Directed Techniques for Improved GPU Register File Utilization. Transactions on Architecture and Code Optimization, 2018, 15, 1-23.	1.6	5
66	GCH: Hints for Triggering Garbage Collections. Lecture Notes in Computer Science, 2007, , 74-94.	1.0	5
67	Compilation and virtualization in the HiPEAC vision. , 2010, , .		5
68	Extending the Î¼Log Framework with Local and Conditional Blackboard Operations. Journal of Symbolic Computation, 1996, 21, 669-697.	0.5	4
69	Process-based parallel logic programming: A survey of the basic issues. Journal of Systems and Software, 1997, 39, 71-82.	3.3	4
70	On the use of subword parallelism in medical image processing. Parallel Computing, 1998, 24, 1537-1556.	1.3	4
71	Speeding Up Architectural Simulations for High-Performance Processors. Simulation, 2004, 80, 451-468.	1.1	4
72	Offline Phase Analysis and Optimization for Multi-configuration Processors. Lecture Notes in Computer Science, 2005, , 202-211.	1.0	4

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73	64-bit versus 32-bit Virtual Machines for Java. Software - Practice and Experience, 2006, 36, 1-26.	2.5	4
74	Evaluation of dynamic binary translation techniques for full system virtualisation on ARMv7-A. Journal of Systems Architecture, 2016, 65, 30-45.	2.5	4
75	Using Decision Trees to Improve Program-Based and Profile-Based Static Branch Prediction. Lecture Notes in Computer Science, 2005, , 336-352.	1.0	4
76	Mitigating Smart Card Fault Injection with Link-Time Code Rewriting: A Feasibility Study. Lecture Notes in Computer Science, 2013, , 221-229.	1.0	4
77	JiTI. Computer Architecture News, 2001, 29, 43-54.	2.5	4
78	Combining Global Code and Data Compaction. ACM SIGPLAN Notices, 2001, 36, 29-38.	0.2	3
79	Highly accurate and efficient evaluation of randomising set index functions. Journal of Systems Architecture, 2003, 48, 429-452.	2.5	3
80	On the side-effects of code abstraction. ACM SIGPLAN Notices, 2003, 38, 244-253.	0.2	3
81	Bidirectional liveness analysis, or how less than half of the Alphaâ€™s registers are used. Journal of Systems Architecture, 2006, 52, 535-548.	2.5	3
82	Calling hardware procedures in a reconfigurable accelerator using RPC-FPGA. , 2017, , .		3
83	Comparing Low-Level Behavior of SPEC CPU and Java Workloads. Lecture Notes in Computer Science, 2005, , 669-679.	1.0	3
84	Constructing Optimal XOR-Functions to Minimize Cache Conflict Misses. Lecture Notes in Computer Science, 2008, , 261-272.	1.0	3
85	ESTIMATING IPC OF A BLOCK STRUCTURED INSTRUCTION SET ARCHITECTURE IN AN EARLY DESIGN STAGE. , 2000, , .		3
86	Sifting out the mud. ACM SIGPLAN Notices, 2002, 37, 275-291.	0.2	3
87	On Delphi lemmas and other memoing techniques for deterministic logic programs. The Journal of Logic Programming, 1997, 30, 145-163.	1.9	2
88	TARILAN: an embedded functional data processing language. Journal of Systems and Software, 1998, 43, 93-102.	3.3	2
89	JiTI: Tracing Memory References for Data Race Detection. Advances in Parallel Computing, 1998, 12, 327-334.	0.3	2
90	Bounding the number of segment histories during data race detection. Parallel Computing, 2002, 28, 1221-1238.	1.3	2

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91	System-wide compaction and specialization of the linux kernel. ACM SIGPLAN Notices, 2005, 40, 95-104.	0.2	2
92	Using hpm-sampling to drive dynamic compilation. ACM SIGPLAN Notices, 2007, 42, 553-568.	0.2	2
93	Implicit hints: Embedding hint bits in programs without ISA changes. , 2010, , .		2
94	Introduction to the special issue on high-performance and embedded architectures and compilers. Transactions on Architecture and Code Optimization, 2012, 8, 1-2.	1.6	2
95	Effective and efficient Javaâ€type obfuscation. Software - Practice and Experience, 2020, 50, 136-160.	2.5	2
96	Object-Relative Addressing: Compressed Pointers in 64-Bit Java Virtual Machines. Lecture Notes in Computer Science, 2007, , 79-100.	1.0	2
97	Early design stage exploration of fixed-length block structured architectures. Journal of Systems Architecture, 2000, 46, 1469-1486.	2.5	1
98	Quantifying behavioral differences between multimedia and general-purpose workloads. Journal of Systems Architecture, 2003, 48, 199-220.	2.5	1
99	Evaluation of the Gini-index for Studying Branch Prediction Features. AIP Conference Proceedings, 2004, , .	0.3	1
100	On Generating Set Index Functions for Randomized Caches. Computer Journal, 2004, 47, 245-258.	1.5	1
101	How accurate should early design stage power/performance tools be? A case study with statistical simulation. Journal of Systems and Software, 2004, 73, 45-62.	3.3	1
102	Optimal sample length for efficient cache simulation. Journal of Systems Architecture, 2005, 51, 513-525.	2.5	1
103	An Analysis of Program Phase Behavior and its Predictability. AIP Conference Proceedings, 2006, , .	0.3	1
104	Clustered indexing for branch predictors. Microprocessors and Microsystems, 2007, 31, 168-177.	1.8	1
105	A Comparative Study of Redundancy in Trace Caches. Lecture Notes in Computer Science, 2002, , 512-516.	1.0	1
106	Nonuniform behavior in instruction traces for contemporary processors. AIP Conference Proceedings, 2001, , .	0.3	0
107	Efficient Architectural Design of High Performance Microprocessors. Advances in Computers, 2004, 61, 45-106.	1.2	0
108	Low-level behavioral analysis of the JVT/AVC decoder. , 2004, 5308, 1371.		0

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109	Improved composite confidence mechanisms for a perceptron branch predictor. Journal of Systems Architecture, 2006, 52, 143-151.	2.5	0
110	Upcoming Computing System Challenges â€“ The HiPEAC Vision Anstehende Herausforderungen der Computer Industrie â€“ Die HiPEAC Vision. IT - Information Technology, 2008, 50, 285-292.	0.6	0
111	A Comparison of Locality-Based and Recency-Based Replacement Policies. Lecture Notes in Computer Science, 2000, , 310-318.	1.0	0
112	INCREASING THE EFFICIENCY OF VALUE PREDICTION IN FUTURE PROCESSORS BY PREDICTING LESS. , 2000, , .		0
113	Independent Hashing as Confidence Mechanism for Value Predictors in Microprocessors. Lecture Notes in Computer Science, 2002, , 458-467.	1.0	0
114	Linux Kernel Compaction through Cold Code Swapping. Lecture Notes in Computer Science, 2009, , 173-200.	1.0	0
115	HiPEAC. Communications of the ACM, 2019, 62, 42-42.	3.3	0