

Armando F Astarloa

List of Publications by Year in descending order

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88
papers

870
citations

567144

15
h-index

610775

24
g-index

90
all docs

90
docs citations

90
times ranked

969
citing authors

#	ARTICLE	IF	CITATIONS
1	Using Software Defined Networking to manage and control IEC 61850-based systems. Computers and Electrical Engineering, 2015, 43, 142-154.	3.0	69
2	Cyber-security in substation automation systems. Renewable and Sustainable Energy Reviews, 2016, 54, 1552-1562.	8.2	55
3	Malguki: an RSSI based ad hoc location algorithm. Microprocessors and Microsystems, 2004, 28, 403-409.	1.8	53
4	Smart Sensor: SoC Architecture for the Industrial Internet of Things. IEEE Internet of Things Journal, 2019, 6, 6567-6577.	5.5	33
5	Implementation of a modified Fuzzy C-Means clustering algorithm for real-time applications. Microprocessors and Microsystems, 2005, 29, 375-380.	1.8	31
6	A novel SEU, MBU and SHE handling strategy for Xilinx Virtex-4 FPGAs. , 2009, , .		31
7	FPGA technology for multi-axis control systems. Mechatronics, 2009, 19, 258-268.	2.0	29
8	PRP and HSR for High Availability Networks in Power Utility Automation: A Method for Redundant Frames Discarding. IEEE Transactions on Smart Grid, 2015, 6, 2325-2332.	6.2	27
9	IEEE 802.1AS Clock Synchronization Performance Evaluation of an Integrated Wired-Wireless TSN Architecture. IEEE Transactions on Industrial Informatics, 2022, 18, 2986-2999.	7.2	25
10	Neuro semantic thresholding using OCR software for high precision OCR applications. Image and Vision Computing, 2010, 28, 571-578.	2.7	22
11	Overview of FPGA-Based Multiprocessor Systems. , 2009, , .		21
12	Synchronization of faulty processors in coarse-grained TMR protected partially reconfigurable FPGA designs. Reliability Engineering and System Safety, 2016, 151, 1-9.	5.1	21
13	Compact and Fast Fault Injection System for Robustness Measurements on SRAM-Based FPGAs. IEEE Transactions on Industrial Electronics, 2014, 61, 2493-2503.	5.2	20
14	Tornado: A self-reconfiguration control system for core-based multiprocessor CSoPCs. Journal of Systems Architecture, 2007, 53, 629-643.	2.5	19
15	Reconfigurable Multiprocessor Systems: A Review. International Journal of Reconfigurable Computing, 2010, 2010, 1-10.	0.2	19
16	On the Utilization of System-on-Chip Platforms to Achieve Nanosecond Synchronization Accuracies in Substation Automation Systems. IEEE Transactions on Smart Grid, 2017, 8, 1932-1942.	6.2	19
17	Cyber-Physical Production System Gateway Based on a Programmable SoC Platform. IEEE Access, 2017, 5, 20408-20417.	2.6	18
18	Security mechanisms to protect IEEE 1588 synchronization: State of the art and trends. , 2015, , .		16

#	ARTICLE	IF	CITATIONS
19	A Survey on Vulnerabilities and Countermeasures in the Communications of the Smart Grid. Electronics (Switzerland), 2021, 10, 1881.	1.8	15
20	Design of a Master Device for the Multifunction Vehicle Bus. IEEE Transactions on Vehicular Technology, 2007, 56, 3695-3708.	3.9	13
21	IEEE 1588 Transparent Clock architecture for FPGA-based network devices. , 2013, , .		13
22	Intelligent gateway for Industry 4.0-compliant production. , 2016, , .		13
23	A Fixed-Latency Architecture to Secure GOOSE and Sampled Value Messages in Substation Systems. IEEE Access, 2021, 9, 51646-51658.	2.6	13
24	Fast and accurate SEU-tolerance characterization method for Zynq SoCs. , 2014, , .		12
25	Estimating the SEU failure rate of designs implemented in FPGAs in presence of MCUs. Microelectronics Reliability, 2017, 78, 85-92.	0.9	12
26	Multiprocessor SoPC-Core for FAT volume computation. Microprocessors and Microsystems, 2005, 29, 421-434.	1.8	11
27	High availability automation networks: PRP and HSR ring implementations. , 2012, , .		11
28	Hardware architecture for a general regression neural network coprocessor. Neurocomputing, 2007, 71, 78-87.	3.5	10
29	An automatic experimental set-up for robustness analysis of designs implemented on SRAM FPGAs. , 2011, , .		9
30	Robustness of different TMR granularities in shared wishbone architectures on SRAM FPGA. , 2012, , .		9
31	Availability Improvement of Layer 2 Seamless Networks Using OpenFlow. Scientific World Journal, The, 2015, 2015, 1-14.	0.8	9
32	Performance Enhancement of High-Availability Seamless Redundancy (HSR) Networks Using OpenFlow. IEEE Communications Letters, 2016, 20, 364-367.	2.5	9
33	GPS-less location algorithm for wireless sensor networks. Computer Communications, 2007, 30, 2904-2916.	3.1	8
34	I2Csec: A secure serial Chip-to-Chip communication protocol. Journal of Systems Architecture, 2011, 57, 206-213.	2.5	8
35	SHA-3 based Message Authentication Codes to secure IEEE 1588 synchronization systems. , 2013, , .		8
36	FPGA implemented cut-through vs store-and-forward switches for reliable ethernet networks. , 2014, , .		8

#	ARTICLE	IF	CITATIONS
37	CPPS Gateway - Implementation of Modbus and Profibus on a SoC programmable platform. IEEE Latin America Transactions, 2018, 16, 335-341.	1.2	8
38	Reconfigurable microstepping control of stepper motors using FPGA embedded RAM. , 0, , .		7
39	Simulink/Modelsim Simulabel VHDL PID Core for Industrial SoPC Multiaxis Controllers. Industrial Electronics Society (IECON), Annual Conference of IEEE, 2006, , .	0.0	7
40	PRP and HSR version 1 (IEC 62439-3 Ed.2), improvements and a prototype implementation. , 2013, , .		7
41	FTL-CFree: A Fuzzy Real-Time Language for Runtime Verification. IEEE Transactions on Industrial Informatics, 2014, 10, 1670-1683.	7.2	7
42	A reconfigurable SoC architecture for high volume and multichannel data transaction in industrial environments. , 0, , .		6
43	Robustness Analysis of Different AES Implementations on SRAM Based FPGAs. , 2011, , .		6
44	Cost-effective redundancy for ethernet train communications using HSR. , 2014, , .		6
45	Using OpenFlow to control redundant paths in wireless networks. Network Protocols and Algorithms, 2016, 8, 90.	1.0	6
46	Fast and accurate Single Bit Error injection into SRAM Based FPGAs. , 2012, , .		5
47	Managing path diversity in layer 2 critical networks by using OpenFlow. , 2015, , .		5
48	MACsec Layer 2 Security in HSR Rings in Substation Automation Systems. Energies, 2017, 10, 162.	1.6	5
49	Secure Protocol and IP Core for Configuration of Networking Hardware IPs in the Smart Grid. Energies, 2018, 11, 510.	1.6	5
50	Multi-architectural 128 bit AES-CBC Core based on Open-Source Hardware AES Implementations for Secure Industrial Communications. , 2006, , .		4
51	Duplicate and circulating frames discard methods for PRP and HSR (IEC62439-3). , 2013, , .		4
52	Securing IEEE 1588 messages with message authentication codes based on the KECCAK cryptographic algorithm implemented in FPGAs. , 2014, , .		4
53	FPGA based nodes for sub-microsecond synchronization of cyber-physical production systems on high availability ring networks. , 2015, , .		4
54	System-on-Programmable-Chip AES-GCM implementation for wire-speed cryptography for SAS. , 2018, , .		4

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55	A Self-Reconfiguration Framework for Multiprocessor CSoPCs. Lecture Notes in Computer Science, 2004, , 1124-1126.	1.0	4
56	Core-Based Reusable Architecture for Slave Circuits with Extensive Data Exchange Requirements. Lecture Notes in Computer Science, 2003, , 497-506.	1.0	4
57	AES-Galois Counter Mode Encryption/Decryption FPGA Core for Industrial and Residential Gigabit Ethernet Communications. Lecture Notes in Computer Science, 2009, , 312-317.	1.0	4
58	OSCRYB: Open Source CRYpto-Bridge for Secure Ethernet point-to-point Industrial Communications. , 2007, , .		3
59	Decompression dual core for SoPC applications in high speed FPGA. , 2007, , .		3
60	FPGA solution for matrix converter double sided space vector modulation algorithm. International Journal of Electronics, 2008, 95, 1181-1200.	0.9	3
61	SoPC Implementation of the TP-KNX Protocol for Domotic Applications. , 2008, , .		3
62	Known-blocking. Synchronization method for reliable processor using TMR & DPR in SRAM FPGAs. , 2011, , .		3
63	Nanosecond accuracy using SoC platforms. , 2014, , .		3
64	High Throughput Serpent Encryption Implementation. Lecture Notes in Computer Science, 2004, , 996-1000.	1.0	2
65	A Reconfigurable Platform to Drive High Frequency Class S Power Amplifiers Using Multi-gigabit Transceivers. , 2008, , .		2
66	PCIREX: A Fast Prototyping Platform for TMR Dynamically Reconfigurable Systems. , 2009, , .		2
67	1588-aware High-Availability Cyber-Physical Production Systems. , 2015, , .		2
68	Synchronizing NTP Referenced SCADA Systems Interconnected by High-availability Networks. , 2020, , .		2
69	Secure Critical Traffic of the Electric Sector over Time-Sensitive Networking. , 2020, , .		2
70	High-Performance Computing Architecture for Sample Value Processing in the Smart Grid. IEEE Access, 2022, 10, 12208-12218.	2.6	2
71	Run-Time Reconfigurable Hardware-Software Architecture for PID Motor Control IP Cores. , 2006, , .		1
72	Configurable-System-on-Programmable-Chip for Power Electronics Control Applications. , 2008, , .		1

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73	DNAX-BCU: An Un-clonable Cost-conscious SoPC Implementation for Bus Coupling Units of the European Installation Bus. , 2009, , .		1
74	A versatile FPGA demonstration platform for academic use. , 2014, , .		1
75	Secure Ethernet Point-to-Point Links for Autonomous Electronic Ballot Boxes. Lecture Notes in Computer Science, 2008, , 603-614.	1.0	1
76	An Autonomous Fault Tolerant System for CAN Communications. Lecture Notes in Computer Science, 2010, , 281-290.	1.0	1
77	Embedded firewall for on-chip bus transactions. Computers and Electrical Engineering, 2022, 98, 107707.	3.0	1
78	Simulation Platform for Architectural Verification and Performance Analysis in Core-Based SoC Design. Lecture Notes in Computer Science, 2004, , 965-969.	1.0	0
79	Modifying Slots in Test Vectors to Validate Decoders of a Train Network. , 2006, , .		0
80	Architecture of a Real-Time Wavelet Transform Calculation SoPC Core for Industrial Applications. Industrial Electronics Society (IECON), Annual Conference of IEEE, 2006, , .	0.0	0
81	High-precision DRM Demodulator for Remote Monitoring. , 2007, , .		0
82	NoCmodel: An extensible framework for Network-on-Chips modeling. , 2011, , .		0
83	On the design of an heuristically optimized multiband spectrum sensing approach for cognitive radio systems. , 2012, , .		0
84	SDR control interface: An FPGA based infrastructure for control of VPX Software Defined Radio systems. , 2013, , .		0
85	Memory requirements analysis for PRP and HSR hardware implementations on FPGAs. , 2013, , .		0
86	System-on-Chip implementation of Reliable Ethernet Networks nodes. , 2013, , .		0
87	Adaptation of IEEE 802.1X for Secure Session Establishment Between Ethernet Peers. Lecture Notes in Computer Science, 2006, , 220-234.	1.0	0
88	Electronic control board for student Rocket. , 2020, , .		0