Wei Deng

List of Publications by Year
in descending order

58 papers	1,204 citations	567281 15 h-index	552781 26 g-index
58 all docs	58 docs citations	58 times ranked	1027 citing authors

#	Article	IF	Citations
1	Class-C VCO With Amplitude Feedback Loop for Robust Start-Up and Enhanced Oscillation Swing. IEEE Journal of Solid-State Circuits, 2013, 48, 429-440.	5.4	151
2	A Compact, Low-Power and Low-Jitter Dual-Loop Injection Locked PLL Using All-Digital PVT Calibration. IEEE Journal of Solid-State Circuits, 2014, 49, 50-60.	5.4	137
3	A Fully Synthesizable All-Digital PLL With Interpolative Phase Coupled Oscillator, Current-Output DAC, and Fine-Resolution Digital Varactor Using Gated Edge Injection Technique. IEEE Journal of Solid-State Circuits, 2015, 50, 68-80.	5.4	117
4	A Sub-Harmonic Injection-Locked Quadrature Frequency Synthesizer With Frequency Calibration Scheme for Millimeter-Wave TDD Transceivers. IEEE Journal of Solid-State Circuits, 2013, 48, 1710-1720.	5.4	100
5	A Fractional-<italic>N</italic> Sub-Sampling PLL using a Pipelined Phase-Interpolator With an FoM of -250ÂdB. IEEE Journal of Solid-State Circuits, 2016, 51, 1630-1640.	5.4	85
6	A Low-Power Low-Noise mm-Wave Subsampling PLL Using Dual-Step-Mixing ILFD and Tail-Coupling Quadrature Injection-Locked Oscillator for IEEE 802.11ad. IEEE Journal of Solid-State Circuits, 2016, 51, 1246-1260.	5.4	85
7	A CMOS 76â€“81-GHz 2-TX 3-RX FMCW Radar Transceiver Based on Mixed-Mode PLL Chirp Generator. IEEE Journal of Solid-State Circuits, 2020, 55, 233-248.	5.4	57
8	A 2.2 GHz -242 dB-FOM 4.2 mW ADC-PLL Using Digital Sub-Sampling Architecture. IEEE Journal of Solid-State Circuits, 2016, 51, 1385-1397.	5.4	43
9	A Sub-mW Fractional-<inline-formula> <tex-math notation="LaTeX">${N}$ </tex-math> </inline-formula> ADPLL With FOM of â^'246 dB for IoT Applications. IEEE Journal of Solid-State Circuits, 2018, 53, 3540-3552.	5.4	42
10	A DPLL-Centric Bluetooth Low-Energy Transceiver With a 2.3-mW Interference-Tolerant Hybrid-Loop Receiver in 65-nm CMOS. IEEE Journal of Solid-State Circuits, 2018, 53, 3672-3687.	5.4	31
11	A 265-mu W Fractional-${N}$ Digital PLL With Seamless Automatic Switching Sub-Sampling/Sampling Feedback Path and Duty-Cycled Frequency-Locked Loop in 65-nm CMOS. IEEE Journal of Solid-State Circuits, 2019, 54, 3478-3492.	5.4	29
12	A Fully Synthesizable Fractional-N MDLL With Zero-Order Interpolation-Based DTC Nonlinearity Calibration and Two-Step Hybrid Phase Offset Calibration. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 603-616.	5.4	27
13	A 60-GHz sub-sampling frequency synthesizer using sub-harmonic injection-locked quadrature oscillators. , 2014, , .		24
14	A Compact and Low-Power Fractionally Injection-Locked Quadrature Frequency Synthesizer Using a Self-Synchronized Gating Injection Technique for Software-Defined Radios. IEEE Journal of Solid-State Circuits, 2014, 49, 1984-1994.	5.4	24
15	A 77-GHz Mixed-Mode FMCW Generator Based on a Vernier TDC With Dual Rising-Edge Fractional-Phase Detector. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 60-73.	5.4	22
16	An Energy-Efficient 10-Gb/s CMOS Millimeter-Wave Transceiver With Direct-Modulation Digital Transmitter and I/Q Phase-Coupled Frequency Synthesizer. IEEE Journal of Solid-State Circuits, 2020, 55, 2027-2042.	5.4	21
17	A feedback class-C VCO with robust startup condition over PVT variations and enhanced oscillation swing. , 2011, , .		20
18	A 13.2% locking-range divide-by-6, 3.1mW, ILFD using even-harmonic-enhanced direct injection technique for millimeter-wave PLLs. , 2013, , .		16

#	Article	IF	Citations
19	A 1.2ps-jitter fully-synthesizable fully-calibrated fractional-N injection-locked PLL using true arbitrary nonlinearity calibration technique. , 2018, , .		16
20	An 8.2-to-21.5 GHz Dual-Core Quad-Mode Orthogonal-Coupled VCO with Concurrently Dual-Output using Parallel 8-Shaped Resonator. , 2021, , .		15
21	A 35-GHz TX and RX Front End With High TX Output Power for Ka-Band FMCW Phased-Array Radar Transceivers in CMOS Technology. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 2089-2098.	3.1	14
22	An HDL-described Fully-synthesizable Sub-GHz IoT Transceiver with Ring Oscillator based Frequency Synthesizer and Digital Background EVM Calibration. , 2019, , .		13
23	A 0.4-ps-Jitter â˜’52-dBc-Spur Synthesizable Injection-Locked PLL With Self-Clocked Nonoverlap Update and Slope-Balanced Subsampling BBPD. IEEE Solid-State Circuits Letters, 2019, 2, 5-8.	2.0	12
24	A 0.5-V, 0.05-to-3.2 GHz, 4.1-to-6.4 GHz LC-VCO using E-TSPC frequency divider with forward body bias for sub-picosecond-jitter clock generation. , 2010, , .		9
25	A current-reuse Class-C LC-VCO with an adaptive bias scheme. , 2013, , .		9
26	A 0.85mm² BLE Transceiver Using an On-Chip Harmonic-Suppressed RFIO Circuitry With T/R Switch. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 196-209.	5.4	8
27	A 58.1-to-65.0GHz frequency synthesizer with background calibration for millimeter-wave TDD transceivers. , 2012, , .		7
28	A D-Band Joint Radar-Communication CMOS Transceiver. IEEE Journal of Solid-State Circuits, 2023, 58, 411-427.	5.4	6
29	A 25MHz–6.44GHz LC-VCO using a 5-port inductor for multi-band frequency generation. , 2011, , .		5
30	A tail-feedback VCO with self-adjusting current modulation scheme. , 2014, , .		5
31	A 0.85mm² BLE Transceiver with Embedded T/R Switch, 2.6mW Fully-Passive Harmonic Suppressed Transmitter and 2.3mW Hybrid-Loop Receiver. , 2018, , .		5
32	A 0.011 mm² PVT-robust fully-synthesizable CDR with a data rate of 10.05 Gb/s in 28nm FD SOI. , 2014, , .		4
33	A pulse-driven LC-VCO with a figure-of-merit of −192dBc/Hz. , 2014, , .		4
34	An LC-DCO based synthesizable injection-locked PLL with an FoM of â˜’250.3dB. , 2016, , .		4
35	A U-Band PLL Using Implicit Distributed Resonators for Sub-THz Wireless Transceivers in 40 nm CMOS. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 1574-1578.	3.0	4
36	A Self-Adapted Two-Point Modulation Type-II Digital PLL for Fast Chirp Rate and Wide Chirp-Bandwidth FMCW Signal Generation. IEEE Journal of Solid-State Circuits, 2022, 57, 1162-1174.	5.4	4

#	Article	IF	Citations
37	A 0.38 mm², 10mhz-6.6 GHz quadrature frequency synthesizer using fractional-N injection-locked technique. , 2012, , .		3
38	A dual-loop injection-locked PLL with all-digital background calibration system for on-chip clock generation. , 2014, , .		3
39	A fully synthesizable injection-locked PLL with feedback current output DAC in 28 nm FDSOI. IEICE Electronics Express, 2015, 12, 20150531-20150531.	0.8	3
40	A fractional-N sub-sampling PLL using a pipelined phase-interpolator with a FoM of −246dB. , 2015, , .		3
41	Silicon-based FMCW signal generators: A review. Journal of Semiconductors, 2020, 41, 111401.	3.7	3
42	A 4.4-GHz 193.2-dB FoM 8-Shaped-Inductor Based LC-VCO Using Orthogonal-Coupled Triple-Coil Transformer. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 4028-4032.	3.0	3
43	A 11.1-to-14.2 GHz Self-adapted Two-point Modulation Dual-path Type-II Digital PLL Concurrently Achieving 124.7-MHz/Î¼s Chirp Rate and 2.27-GHz Bandwidth. , 2021, , .		2
44	A PVT-robust feedback class-C VCO using an oscillation swing enhancement technique. , 2012, , .		1
45	A 20 GHz push-push voltage-controlled oscillator for a 60 GHz frequency synthesizer. , 2012, , .		1
46	A 0.015-mm² 60-GHz reconfigurable wake-up receiver by reusing multi-stage LNAs. , 2014, , .		1
47	A swing-enhanced current-reuse class-C VCO with dynamic bias control circuits. , 2014, , .		1
48	A 58.3-to-65.4 GHz 34.2 mW sub-harmonically injection-locked PLL with a sub-sampling phase detection. , 2015, , .		1
49	An HDL-synthesized gated-edge-injection PLL with a current output DAC. , 2015, , .		1
50	A 20GHz Push-Push Voltage-Controlled Oscillator Using Second-Harmonic Peaking Technique for a 60GHz Frequency Synthesizer. IEICE Transactions on Electronics, 2013, E96.C, 804-812.	0.6	1
51	A 0.0055mm² 480ÂµW Fully Synthesizable PLL Using Stochastic TDC in 28nm FDSOI. IEICE Transactions on Electronics, 2016, E99.C, 632-640.	0.6	1
52	A 53.1-to-64.5 GHz In-Phase Coupled Quadrature Injection-Locked Oscillator with Transformer-Based I/Q-Phase Differential Injection Scheme. , 2020, , .		1
53	An ultra-low-voltage LC-VCO with a frequency extension circuit for future 0.5-V clock generation. , 2011, , .		0
54	A sub-harmonic injection-locked frequency synthesizer with frequency calibration scheme for use in 60GHz TDD transceivers. , 2013, , .		0

#	Article	IF	Citations
55	A fractional-N harmonic injection-locked frequency synthesizer with 10MHz–6.6GHz quadrature outputs for software-defined radios. , 2013, , .		0
56	A tail-current modulated VCO with adaptive-bias scheme. , 2015, , .		0
57	An HDL-synthesized injection-locked PLL using LC-based DCO for on-chip clock generation. , 2017, , .		0
58	A 0.5-V, 0.05-to-3.2GHz LC-Based Clock Generator for Substituting Ring Oscillators under Low-Voltage Condition. IEICE Transactions on Electronics, 2012, E95.C, 1285-1296.	0.6	0