Levent Aksoy

List of Publications by Year
in descending order

50 papers	472 citations	1040056 9 h-index	940533 16 g-index
51 all docs	51 docs citations	51 times ranked	150 citing authors

#	Article	IF	Citations
1	Exact and Approximate Algorithms for the Optimization of Area and Delay in Multiple Constant Multiplications. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 1013-1026.	2.7	92
2	Search algorithms for the multiple constant multiplications problem: Exact and approximate. Microprocessors and Microsystems, 2010, 34, 151-162.	2.8	75
3	A Tutorial on Multiplierless Design of FIR Filters: Algorithms and Architectures. Circuits, Systems, and Signal Processing, 2014, 33, 1689-1719.	2.0	32
4	An Exact Breadth-First Search Algorithm for the Multiple Constant Multiplications Problem. , 2008, , .		28
5	Design of Digit-Serial FIR Filters: Algorithms, Architectures, and a CAD Tool. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 498-511.	3.1	23
6	Finding the optimal tradeoff between area and delay in multiple constant multiplications. Microprocessors and Microsystems, 2011, 35, 729-741.	2.8	16
7	Optimization Algorithms for the Multiplierless Realization of Linear Transforms. ACM Transactions on Design Automation of Electronic Systems, 2012, 17, 1-27.	2.6	15
8	Exact and Approximate Algorithms for the Filter Design Optimization Problem. IEEE Transactions on Signal Processing, 2015, 63, 142-154.	5.3	12
9	Optimization of Area in Digital FIR Filters using Gate-Level Metrics. Proceedings - Design Automation Conference, 2007, , .	0.0	11
10	Multiplierless Design of Linear DSP Transforms. International Federation for Information Processing, 2012, , 73-93.	0.4	11
11	Optimization of area in digit-serial Multiple Constant Multiplications at gate-level. , 2011, , .		10
12	Optimization of Area and Delay at Gate-Level in Multiple Constant Multiplications. , 2010, , .		9
13	Effect of Number Representation on the Achievable Minimum Number of Operations in Multiple Constant Multiplications. Signal Processing Systems Design and Implementation (siPS), IEEE Workshop on, 2007, , .	0.0	8
14	Efficient shift-adds design of digit-serial multiple constant multiplications. , 2011, , .		8
15	Realization of Four-Terminal Switching Lattices: Technology Development and Circuit Modeling. , 2019, , .		8
16	Minimum number of operations under a general number representation for digital filter synthesis. , 2007, , .		7
17	Design of low-power multiple constant multiplications using low-complexity minimum depth operations. , 2011, , .		7
18	A Satisfiability-Based Approximate Algorithm for Logic Synthesis Using Switching Lattices. , 2019, , .		7

#	Article	IF	Citations
19	Area optimization algorithms in high-speed digital FIR filter synthesis. , 2008, , .		6
20	Multiple tunable constant multiplications. , 2012, , .		6
21	Design of low-complexity digital finite impulse response filters on FPGAs. , 2012, , .		6
22	Multiplierless Design of Folded DSP Blocks. ACM Transactions on Design Automation of Electronic Systems, 2014, 20, 1-24.	2.6	6
23	A novel method for the approximation of multiplierless constant matrix vector multiplication. Eurasip Journal on Embedded Systems, 2016, 2016, .	1.2	6
24	Radix-2 Decimation in Time (DIT) FFT implementation based on a Matrix-Multiple Constant multiplication approach. , 2010, , .		5
25	Efficient design of FIR filters using hybrid multiple constant multiplications on FPGA. , 2014, , .		5
26	Efficient Hardware Implementation of Artificial Neural Networks Using Approximate Multiply-Accumulate Blocks. , 2020, , .		5
27	An approximate algorithm for the multiple constant multiplications problem. , 2008, , .		4
28	High-level algorithms for the optimization of gate-level area in digit-serial multiple constant multiplications. The Integration VLSI Journal, 2012, 45, 294-306.	2.1	4
29	Novel Methods for Efficient Realization of Logic Functions Using Switching Lattices. IEEE Transactions on Computers, 2020, 69, 427-440.	3.4	4
30	Efficient Time-Multiplexed Realization of Feedforward Artificial Neural Networks. , 2020, , .		4
31	Optimization of gate-level area in high throughput Multiple Constant Multiplications. , 2011, , .		3
32	ECHO: A novel method for the multiplierless design of constant array vector multiplication. , 2014, , .		3
33	Approximation of multiple constant multiplications using minimum look-up tables on FPGA. , 2015, , .		3
34	High-level Intellectual Property Obfuscation via Decoy Constants. , 2021, , .		3
35	CMOS Implementation of Switching Lattices. , 2020, , .		3
36	Optimization of area under a delay constraint in digital filter synthesis using SAT-based integer linear programming. , 2006, , .		2

#	Article	IF	Citations
37	A Novel Method for the Approximation of Multiplierless Constant Matrix Vector Multiplication. , 2015, , .		2
38	A Novel Method for the Realization of Complex Logic Functions using Switching Lattices. , 2020, , .		2
39	ASSUMEs: Heuristic Algorithms for Optimization of Area and Delay in Digital Filter Synthesis. , 2006, , .		1
40	Design of low-complexity and high-speed digital Finite Impulse Response filters. , 2010, , .		1
41	A hybrid algorithm for the optimization of area and delay in linear DSP transforms. , 2011, , .		1
42	SIREN. , 2013, , .		1
43	Optimization of design complexity in time-multiplexed constant multiplications. , 2014, , .		1
44	Hardware Obfuscation of Digital FIR Filters. , 2022, , .		1
45	Multiplierless Design of Very Large Constant Multiplications in Cryptography. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 4503-4507.	3.0	1
46	Design of low complexity digital FIR filters. , 2009, , .		0
47	Towards the least complex time-multiplexed constant multiplication. , 2013, , .		0
48	Exploration of tradeoffs in the design of integer cosine transforms for image compression. , 2013, , .		0
49	Technology Development and Modeling of Switching Lattices Using Square and H Shaped Four-Terminal Switches. IEEE Transactions on Emerging Topics in Computing, 2022, 10, 351-360.	4.6	0
50	Realization of Logic Functions Using Switching Lattices Under a Delay Constraint. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 2036-2048.	2.7	0