

# Johannes Partzsch

## List of Publications by Year in descending order

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Version: 2024-02-01

42  
papers

769  
citations

686830

13  
h-index

642321

23  
g-index

42  
all docs

42  
docs citations

42  
times ranked

830  
citing authors

| #  | ARTICLE                                                                                                                                                                         | IF  | CITATIONS |
|----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----------|
| 1  | Neuromorphic hardware in the loop: Training a deep spiking network on the BrainScaleS wafer-scale system. , 2017, , .                                                           |     | 99        |
| 2  | A Biological-Realtime Neuromorphic System in 28 nm CMOS Using Low-Leakage Switched Capacitor Circuits. IEEE Transactions on Biomedical Circuits and Systems, 2016, 10, 243-254. | 2.7 | 77        |
| 3  | A comprehensive workflow for general-purpose neural modeling with highly configurable neuromorphic hardware systems. Biological Cybernetics, 2011, 104, 263-296.                | 0.6 | 72        |
| 4  | Live demonstration: A scaled-down version of the BrainScaleS wafer-scale neuromorphic system. , 2012, , .                                                                       |     | 41        |
| 5  | Analyzing the Scaling of Connectivity in Neuromorphic Hardware and in Models of Neural Networks. IEEE Transactions on Neural Networks, 2011, 22, 919-935.                       | 4.8 | 39        |
| 6  | Memory-Efficient Deep Learning on a SpiNNaker 2 Prototype. Frontiers in Neuroscience, 2018, 12, 840.                                                                            | 1.4 | 38        |
| 7  | VLSI implementation of a 2.8 Gevent/s packet-based AER interface with routing and event sorting functionality. Frontiers in Neuroscience, 2011, 5, 117.                         | 1.4 | 36        |
| 8  | Rate and pulse based plasticity governed by local synaptic state variables. Frontiers in Synaptic Neuroscience, 2010, 2, 33.                                                    | 1.3 | 35        |
| 9  | A 32 GBit/s communication SoC for a waferscale neuromorphic system. The Integration VLSI Journal, 2012, 45, 61-75.                                                              | 1.3 | 30        |
| 10 | Switched-capacitor realization of presynaptic short-term-plasticity and stop-learning synapses in 28 nm CMOS. Frontiers in Neuroscience, 2015, 9, 10.                           | 1.4 | 27        |
| 11 | Plasticity and Adaptation in Neuromorphic Biohybrid Systems. IScience, 2020, 23, 101589.                                                                                        | 1.9 | 26        |
| 12 | Comparing Loihi with a SpiNNaker 2 prototype on low-latency keyword spotting and adaptive robotic control. Neuromorphic Computing and Engineering, 2021, 1, 014002.             | 2.8 | 26        |
| 13 | A Biohybrid Setup for Coupling Biological and Neuromorphic Neural Networks. Frontiers in Neuroscience, 2019, 13, 432.                                                           | 1.4 | 24        |
| 14 | A fixed point exponential function accelerator for a neuromorphic many-core system. , 2017, , .                                                                                 |     | 21        |
| 15 | Efficient Reward-Based Structural Plasticity on a SpiNNaker 2 Prototype. IEEE Transactions on Biomedical Circuits and Systems, 2019, 13, 579-591.                               | 2.7 | 20        |
| 16 | Replicating experimental spike and rate based neural learning in CMOS. , 2010, , .                                                                                              |     | 18        |
| 17 | Accuracy evaluation of numerical methods used in state-of-the-art simulators for spiking neural networks. Journal of Computational Neuroscience, 2012, 32, 309-326.             | 0.6 | 17        |
| 18 | VLSI implementation of a conductance-based multi-synapse using switched-capacitor circuits. , 2014, , .                                                                         |     | 17        |

| #  | ARTICLE                                                                                                                                                                   | IF  | CITATIONS |
|----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----------|
| 19 | A location-independent direct link neuromorphic interface. , 2013, , .                                                                                                    |     | 13        |
| 20 | Reducing the computational footprint for real-time BCPNN learning. Frontiers in Neuroscience, 2015, 9, 2.                                                                 | 1.4 | 13        |
| 21 | Dynamic Power Management for Neuromorphic Many-Core Systems. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 2973-2986.                            | 3.5 | 12        |
| 22 | Configurable analog-digital conversion using the neural engineering framework. Frontiers in Neuroscience, 2014, 8, 201.                                                   | 1.4 | 10        |
| 23 | Synapse dynamics in CMOS derived from a model of neurotransmitter release. , 2011, , .                                                                                    |     | 7         |
| 24 | Developing structural constraints on connectivity for biologically embedded neural networks. Biological Cybernetics, 2012, 106, 191-200.                                  | 0.6 | 6         |
| 25 | Event-based Neural Network for ECG Classification with Delta Encoding and Early Stopping. , 2020, , .                                                                     |     | 6         |
| 26 | A Calibration Technique for Bang-Bang ADPLLs Using Jitter Distribution Monitoring. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 3548-3552. | 2.1 | 5         |
| 27 | The operating system of the neuromorphic BrainScaleS-1 system. Neurocomputing, 2022, 501, 790-810.                                                                        | 3.5 | 5         |
| 28 | Network-driven design principles for neuromorphic systems. Frontiers in Neuroscience, 2015, 9, 386.                                                                       | 1.4 | 4         |
| 29 | Flexible and stretchable redistribution layer with embedded chips for human-machine interface. , 2020, , .                                                                |     | 4         |
| 30 | A pulse communication flow ready for accelerated neuromorphic experiments. , 2014, , .                                                                                    |     | 3         |
| 31 | Dynamic voltage and frequency scaling for neuromorphic many-core systems. , 2017, , .                                                                                     |     | 3         |
| 32 | BCM and Membrane Potential: Alternative Ways to Timing Dependent Plasticity. Lecture Notes in Computer Science, 2009, , 137-144.                                          | 1.0 | 3         |
| 33 | Mapping Deep Neural Networks on SpiNNaker2. , 2020, , .                                                                                                                   |     | 3         |
| 34 | On the Relation between Bursts and Dynamic Synapse Properties: A Modulation-Based Ansatz. Computational Intelligence and Neuroscience, 2009, 2009, 1-13.                  | 1.1 | 2         |
| 35 | Mean Field Approach for Configuring Population Dynamics on a Biohybrid Neuromorphic System. Journal of Signal Processing Systems, 2020, 92, 1303-1321.                    | 1.4 | 2         |
| 36 | Real-time Hardware Implementation of ARM CoreSight Trace Decoder. IEEE Design and Test, 2021, 38, 69-77.                                                                  | 1.1 | 2         |

| #  | ARTICLE                                                                                                         | IF  | CITATIONS |
|----|-----------------------------------------------------------------------------------------------------------------|-----|-----------|
| 37 | Transient responses of activity-dependent synapses to modulated pulse trains. Neurocomputing, 2009, 73, 99-105. | 3.5 | 1         |
| 38 | Live demonstration: Dynamic voltage and frequency scaling for neuromorphic many-core systems. , 2017, , .       |     | 1         |
| 39 | Analyzing ARM CoreSight ETMv4.x Data Trace Stream with a Real-time Hardware Accelerator. , 2021, , .            |     | 1         |
| 40 | Configurable pulse routing architecture for accelerated multi-node neuromorphic systems. , 2014, , .            |     | 0         |
| 41 | Exploration of FPGA architectures for tight coupled accelerators in a 22nm FDSOI technology. , 2017, , .        |     | 0         |
| 42 | Delay-Based Neural Computation: Pulse Routing Architecture and Benchmark Application in FPGA. , 2021, , .       |     | 0         |