Zhiwei Li

List of Publications by Year
in descending order

35	387	1305906 8	1181555 14
papers	citations	h-index	g-index

35	35	35	615
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	AIMCU-MESO: An In-Memory Computing Unit Constructed by MESO Device. ACM Transactions on Design Automation of Electronic Systems, 2023, 28, 1-16.	1.9	0
2	In Situ Learning in Hardware Compatible Multilayer Memristive Spiking Neural Network. IEEE Transactions on Cognitive and Developmental Systems, 2022, 14, 448-461.	2.6	6
3	A training strategy for improving the robustness of memristor-based binarized convolutional neural networks. Semiconductor Science and Technology, 2022, 37, 015013.	1.0	3
4	An Efficient PWL Memristor Model With MMSE Parameter Fitting. IEEE Transactions on Electron Devices, 2022, 69, 1545-1552.	1.6	1
5	Error Detection and Correction Method Toward Fully Memristive Stateful Logic Design. Advanced Intelligent Systems, 2022, 4, .	3.3	5
6	On the Compensation of Timing Mismatch in Two-Channel Time-Interleaved ADCs: Strategies and a Novel Parallel Compensation Structure. IEEE Transactions on Signal Processing, 2022, 70, 2460-2475.	3.2	2
7	Network Pruning Towards Highly Efficient RRAM Accelerator. IEEE Nanotechnology Magazine, 2022, 21, 340-351.	1.1	0
8	Binary Memristive Synapse Based Vector Neural Network Architecture and Its Application. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 772-776.	2.2	2
9	Memristor Based Binary Convolutional Neural Network Architecture With Configurable Neurons. Frontiers in Neuroscience, 2021, 15, 639526.	1.4	23
10	Memristive Stateful Logic with N-Modular Redundancy Error Correction Design towards High Reliability. , 2021, , .		4
11	Logic Implementation Based on Double Memristors. , 2021, , .		0
12	EEG Signal Epilepsy Detection System Based on Convolutional Neural Network and Memristor Array. , 2021, , .		3
13	In-situ learning in multilayer locally-connected memristive spiking neural network. Neurocomputing, 2021, 463, 251-264.	3.5	4
14	Enhanced Spiking Neural Network with forgetting phenomenon based on electronic synaptic devices. Neurocomputing, 2020, 408, 21-30.	3.5	4
15	Solution to alleviate the impact of line resistance on the crossbar array. IET Circuits, Devices and Systems, 2020, 14, 498-504.	0.9	2
16	Implication of unsafe writing on the MAGIC NOR gate. Microelectronics Journal, 2020, 103, 104866.	1.1	12
17	CiMC: A Computing-in-Memory Controller for Memristive Crossbar Array. IOP Conference Series: Materials Science and Engineering, 2020, 768, 052044.	0.3	0
18	Unsafe Writing Impacts on the Stateful Memristor Gates. , 2020, , .		4

#	Article	IF	Citations
19	SCMOS: Series-Connected Memristor-only Stateful Logic. , 2020, , .		0
20	An Efficient PWL Memristor Model Towards Circuit Design. , 2020, , .		0
21	Cases Study of Inputs Split Based Calibration Method for RRAM Crossbar. IEEE Access, 2019, 7, 141792-141800.	2.6	2
22	Understanding the conduction and switching mechanism of Ti/AlOx/TaOx/Pt analog memristor. Physics Letters, Section A: General, Atomic and Solid State Physics, 2019, 383, 125877.	0.9	11
23	A memristor-based convolutional neural network with full parallelization architecture. IEICE Electronics Express, 2019, 16, 20181034-20181034.	0.3	12
24	Quaternary synapses network for memristor-based spiking convolutional neural networks. IEICE Electronics Express, 2019, 16, 20190004-20190004.	0.3	9
25	Instability changes the MAGIC NAND gate to the NOR gate. , 2019, , .		0
26	MAGIC NAND within NOR gate. , 2019, , .		0
27	A TaO_x-Based Electronic Synapse With High Precision for Neuromorphic Computing. IEEE Access, 2019, 7, 184700-184706.	2.6	6
28	Low-Consumption Neuromorphic Memristor Architecture Based on Convolutional Neural Networks. , 2018, , .		8
29	Quasi-Analytical Model of 3-D Vertical-RRAM Array Architecture for MB-Level Design. IEEE Transactions on Electron Devices, 2017, 64, 1568-1574.	1.6	9
30	Design of Ternary Neural Network With 3-D Vertical RRAM Array. IEEE Transactions on Electron Devices, 2017, 64, 2721-2727.	1.6	60
31	New write operation scheme for alleviating effect of line resistance on RRAM crossbar array. , 2016, , .		0
32	Binary neural network with 16 Mb RRAM macro chip for classification and online training. , 2016, , .		154
33	Design Tradeoffs of Vertical RRAM-Based 3-D Cross-Point Array. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 3460-3467.	2.1	36
34	A memristor random circuit breaker model accounting for stimulus thermal accumulation. IEICE Electronics Express, 2016, 13, 20160376-20160376.	0.3	3
35	Cationic Interstitials: An Overlooked Ionic Defect in Memristors. Frontiers in Chemistry, 0, 10, .	1.8	2