Antonios Paschalis

List of Publications by Year
in descending order

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60	937	430754	552653
papers	citations	18	26
		h-index	g-index

60	60	60	452
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Efficient Hardware Architectures and Implementations of Packet-Level Erasure Coding Schemes for High Data Rate Reliable Satellite Communications. IEEE Transactions on Aerospace and Electronic Systems, 2022, 58, 2269-2280.	2.6	2
2	A 3.3 Gbps CCSDS 123.0-B-1 Multispectral & Hyperspectral Image Compression Hardware Accelerator on a Space-Grade SRAM FPGA. IEEE Transactions on Emerging Topics in Computing, 2021, 9, 90-103.	3.2	27
3	High-Performance COTS FPGA SoC for Parallel Hyperspectral Image Compression With CCSDS-123.0-B-1. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 2397-2409.	2.1	17
4	Efficient Architectures for Multigigabit CCSDS LDPC Encoders. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 1118-1127.	2.1	18
5	Analyzing the Resilience to SEUs of an Image Data Compression Core in a COTS SRAM FPGA. , 2019, , .		4
6	Development of ASPIICS: a coronagraph based on Proba-3 formation flying mission. , 2018, , .		20
7	Application-Specific Solutions. , 2018, , 189-216.		1
8	Recent achievements on ASPIICS, an externally occulted coronagraph for PROBA-3. Proceedings of SPIE, 2016, , .	0.8	5
9	An efficient LDPC encoder architecture for space applications. , 2016, , .		15
10	Design status of ASPIICS, an externally occulted coronagraph for PROBA-3. Proceedings of SPIE, 2015, , .	0.8	18
11	Efficient field-programmable gate array implementation of CCSDS 121.0-B-2 lossless data compression algorithm for image compression. Journal of Applied Remote Sensing, 2015, 9, 097499.	0.6	8
12	Dependable Multicore Architectures at Nanoscale: The View From Europe. IEEE Design and Test, 2015, 32, 17-28.	1.1	21
13	A single chip dependable and adaptable payload Data Processing Unit. , 2015, , .		1
14	Software-Based Self-Test for Small Caches in Microprocessors. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2014, 33, 1991-2004.	1.9	20
15	ASPIICS: an externally occulted coronagraph for PROBA-3: Design evolution. Proceedings of SPIE, 2014, , .	0.8	12
16	Dependable reconfigurable space systems: Challenges, new trends and case studies. , 2014, , .		2
17	The Space Weather and Ultraviolet Solar Variability (SWUSV) Microsatellite Mission. Journal of Advanced Research, 2013, 4, 235-251.	4.4	12
18	Online error detection in multiprocessor chips: A test scheduling study. , 2013, , .		4

#	Article	IF	Citations
19	Software-Based Self Test Methodology for On-Line Testing of L1 Caches in Multithreaded Multicore Architectures. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 786-790.	2.1	18
20	Accumulator Based 3-Weight Pattern Generation. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2012, 20, 357-361.	2.1	17
21	Low Energy Online Self-Test of Embedded Processors in Dependable WSN Nodes. IEEE Transactions on Dependable and Secure Computing, 2012, 9, 86-100.	3.7	11
22	Recursive Pseudo-Exhaustive Two-Pattern Generation. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2010, 18, 142-152.	2.1	12
23	Exploiting Thread-Level Parallelism in Functional Self-Testing of CMT Processors. , 2009, , .		14
24	Instruction-Based Online Periodic Self-Testing of Microprocessors with Floating-Point Units. IEEE Transactions on Dependable and Secure Computing, 2009, 6, 124-134.	3.7	10
25	Software-Based Self-Testing of Symmetric Shared-Memory Multiprocessors. IEEE Transactions on Computers, 2009, 58, 1682-1694.	2.4	35
26	Hybrid-SBST Methodology for Efficient Testing of Processor Cores. IEEE Design and Test of Computers, 2008, 25, 64-75.	1.4	59
27	An Input Vector Monitoring Concurrent BIST Architecture Based on a Precomputed Test Set. IEEE Transactions on Computers, 2008, 57, 1012-1022.	2.4	29
28	Systematic Software-Based Self-Test for Pipelined Processors. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2008, 16, 1441-1453.	2.1	79
29	Functional Processor-Based Testing of Communication Peripherals in Systems-on-Chip. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2007, 15, 971-975.	2.1	12
30	Software-Based Self-Testing of Embedded Processors. , 2007, , 447-481.		5
31	Systematic software-based self-test for pipelined processors. , 2006, , .		32
32	Testability Analysis and Scalable Test Generation for High-Speed Floating-Point Units. IEEE Transactions on Computers, 2006, 55, 1449-1457.	2.4	4
33	A Concurrent Built-In Self-Test Architecture Based on a Self-Testing RAM. IEEE Transactions on Reliability, 2005, 54, 69-78.	3.5	33
34	Embedded Processor-Based Self-Test. Frontiers in Electronic Testing, 2004, , .	0.3	36
35	Easily Testable Cellular Carry Lookahead Adders. Journal of Electronic Testing: Theory and Applications (JETTA), 2003, 19, 285-298.	0.9	17
36	Instruction-Based Self-Testing of Processor Cores. Journal of Electronic Testing: Theory and Applications (JETTA), 2003, 19, 103-112.	0.9	30

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37	An Effective Deterministic BIST Scheme for Shifter/Accumulator Pairs in Datapaths. Journal of Electronic Testing: Theory and Applications (JETTA), 2001, 17, 97-107.	0.9	3
38	Sequential fault modeling and test pattern generation for CMOS iterative logic arrays. IEEE Transactions on Computers, 2000, 49, 1083-1099.	2.4	22
39	On robust two-pattern testing of one-dimensional CMOS iterative logic arrays. International Journal of Electronics, 1999, 86, 967-978.	0.9	0
40	An Accumulator-Based BIST Approach for Two-Pattern Testing. Journal of Electronic Testing: Theory and Applications (JETTA), 1999, 15, 267-278.	0.9	9
41	An effective built-in self-test scheme for parallel multipliers. IEEE Transactions on Computers, 1999, 48, 936-950.	2.4	40
42	Concurrent Delay Testing in Totally Self-Checking Systems. Journal of Electronic Testing: Theory and Applications (JETTA), 1998, 12, 55-61.	0.9	4
43	Title is missing!. Journal of Electronic Testing: Theory and Applications (JETTA), 1998, 13, 315-319.	0.9	14
44	Testable designs of one-count generators. International Journal of Electronics, 1998, 85, 629-650.	0.9	0
45	Hierarchical robust test generation for CMOS circuit stuck-open faults. International Journal of Electronics, 1997, 82, 45-60.	0.9	0
46	An efficient built-in self test method for robust path delay fault testing. Journal of Electronic Testing: Theory and Applications (JETTA), 1996, 8, 219-222.	0.9	25
47	C-Testable modified-Booth multipliers. Journal of Electronic Testing: Theory and Applications (JETTA), 1996, 8, 241-260.	0.9	13
48	Testing CMOS combinational iterative logic arrays for realistic faults. The Integration VLSI Journal, 1996, 21, 209-228.	1.3	5
49	Fast C-testable array multipliers. International Journal of Electronics, 1996, 80, 561-582.	0.9	4
50	Robust test generation for transistor stuck-open faults in CMOS complex gates. International Journal of Electronics, 1995, 79, 129-142.	0.9	3
51	Efficient totally self-checking checkers for a class of Borden codes. IEEE Transactions on Computers, 1995, 44, 1318-1322.	2.4	8
52	On TSC checkers for m-out-of-n codes. IEEE Transactions on Computers, 1995, 44, 1055-1059.	2.4	12
53	Totally self-checking checkers for Borden codes. International Journal of Electronics, 1994, 76, 57-64.	0.9	8
54	Efficient structured design of totally self-checking A/-out-of-/V code checkers with N>2M and M=2^kâ˜'1. International Journal of Electronics, 1994, 77, 251-257.	0.9	5

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55	Efficient PL A design of TSC 1-out-of-ncode checkers. International Journal of Electronics, 1992, 73, 471-484.	0.9	5
56	Fast and low cost TSC checkers for 1-out-of-nand (n- l)-out-of-ncodes in MOS transistor implementation. International Journal of Electronics, 1991, 71, 781-791.	0.9	8
57	An efficient TSC 1-out-of-3 code checker. IEEE Transactions on Computers, 1990, 39, 407-411.	2.4	16
58	Efficient modular design of TSC checkers for m-out-of-2m codes. IEEE Transactions on Computers, 1988, 37, 301-309.	2.4	34
59	Efficient design of totally self-checking checkers for all low-cost arithmetic codes. IEEE Transactions on Computers, 1988, 37, 807-814.	2.4	38
60	Concurrently totally self-checking microprogram control unit with duplication of microprogram sequencer. Microprocessing and Microprogramming, 1987, 20, 271-281.	0.3	1