

# Antonios Paschalis

## List of Publications by Year in descending order

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60  
papers

937  
citations

430754

18  
h-index

552653

26  
g-index

60  
all docs

60  
docs citations

60  
times ranked

452  
citing authors

#	ARTICLE	IF	CITATIONS
1	Systematic Software-Based Self-Test for Pipelined Processors. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2008, 16, 1441-1453.	2.1	79
2	Hybrid-SBST Methodology for Efficient Testing of Processor Cores. IEEE Design and Test of Computers, 2008, 25, 64-75.	1.4	59
3	An effective built-in self-test scheme for parallel multipliers. IEEE Transactions on Computers, 1999, 48, 936-950.	2.4	40
4	Efficient design of totally self-checking checkers for all low-cost arithmetic codes. IEEE Transactions on Computers, 1988, 37, 807-814.	2.4	38
5	Embedded Processor-Based Self-Test. Frontiers in Electronic Testing, 2004, , .	0.3	36
6	Software-Based Self-Testing of Symmetric Shared-Memory Multiprocessors. IEEE Transactions on Computers, 2009, 58, 1682-1694.	2.4	35
7	Efficient modular design of TSC checkers for m-out-of-2m codes. IEEE Transactions on Computers, 1988, 37, 301-309.	2.4	34
8	A Concurrent Built-In Self-Test Architecture Based on a Self-Testing RAM. IEEE Transactions on Reliability, 2005, 54, 69-78.	3.5	33
9	Systematic software-based self-test for pipelined processors. , 2006, , .		32
10	Instruction-Based Self-Testing of Processor Cores. Journal of Electronic Testing: Theory and Applications (JETTA), 2003, 19, 103-112.	0.9	30
11	An Input Vector Monitoring Concurrent BIST Architecture Based on a Precomputed Test Set. IEEE Transactions on Computers, 2008, 57, 1012-1022.	2.4	29
12	A 3.3 Gbps CCSDS 123.0-B-1 Multispectral & Hyperspectral Image Compression Hardware Accelerator on a Space-Grade SRAM FPGA. IEEE Transactions on Emerging Topics in Computing, 2021, 9, 90-103.	3.2	27
13	An efficient built-in self test method for robust path delay fault testing. Journal of Electronic Testing: Theory and Applications (JETTA), 1996, 8, 219-222.	0.9	25
14	Sequential fault modeling and test pattern generation for CMOS iterative logic arrays. IEEE Transactions on Computers, 2000, 49, 1083-1099.	2.4	22
15	Dependable Multicore Architectures at Nanoscale: The View From Europe. IEEE Design and Test, 2015, 32, 17-28.	1.1	21
16	Software-Based Self-Test for Small Caches in Microprocessors. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2014, 33, 1991-2004.	1.9	20
17	Development of ASPIICS: a coronagraph based on Proba-3 formation flying mission. , 2018, , .		20
18	Software-Based Self Test Methodology for On-Line Testing of L1 Caches in Multithreaded Multicore Architectures. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 786-790.	2.1	18

#	ARTICLE	IF	CITATIONS
19	Design status of ASPIICS, an externally occulted coronagraph for PROBA-3. Proceedings of SPIE, 2015, , .	0.8	18
20	Efficient Architectures for Multigigabit CCSDS LDPC Encoders. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 1118-1127.	2.1	18
21	Easily Testable Cellular Carry Lookahead Adders. Journal of Electronic Testing: Theory and Applications (JETTA), 2003, 19, 285-298.	0.9	17
22	Accumulator Based 3-Weight Pattern Generation. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2012, 20, 357-361.	2.1	17
23	High-Performance COTS FPGA SoC for Parallel Hyperspectral Image Compression With CCSDS-123.0-B-1. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 2397-2409.	2.1	17
24	An efficient TSC 1-out-of-3 code checker. IEEE Transactions on Computers, 1990, 39, 407-411.	2.4	16
25	An efficient LDPC encoder architecture for space applications. , 2016, , .		15
26	Title is missing!. Journal of Electronic Testing: Theory and Applications (JETTA), 1998, 13, 315-319.	0.9	14
27	Exploiting Thread-Level Parallelism in Functional Self-Testing of CMT Processors. , 2009, , .		14
28	C-Testable modified-Booth multipliers. Journal of Electronic Testing: Theory and Applications (JETTA), 1996, 8, 241-260.	0.9	13
29	On TSC checkers for m-out-of-n codes. IEEE Transactions on Computers, 1995, 44, 1055-1059.	2.4	12
30	Functional Processor-Based Testing of Communication Peripherals in Systems-on-Chip. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2007, 15, 971-975.	2.1	12
31	Recursive Pseudo-Exhaustive Two-Pattern Generation. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2010, 18, 142-152.	2.1	12
32	The Space Weather and Ultraviolet Solar Variability (SWUSV) Microsatellite Mission. Journal of Advanced Research, 2013, 4, 235-251.	4.4	12
33	ASPIICS: an externally occulted coronagraph for PROBA-3: Design evolution. Proceedings of SPIE, 2014, , .	0.8	12
34	Low Energy Online Self-Test of Embedded Processors in Dependable WSN Nodes. IEEE Transactions on Dependable and Secure Computing, 2012, 9, 86-100.	3.7	11
35	Instruction-Based Online Periodic Self-Testing of Microprocessors with Floating-Point Units. IEEE Transactions on Dependable and Secure Computing, 2009, 6, 124-134.	3.7	10
36	An Accumulator-Based BIST Approach for Two-Pattern Testing. Journal of Electronic Testing: Theory and Applications (JETTA), 1999, 15, 267-278.	0.9	9

#	ARTICLE	IF	CITATIONS
37	Fast and low cost TSC checkers for 1-out-of- $n$ and $(n-1)$ -out-of- $n$ codes in MOS transistor implementation. International Journal of Electronics, 1991, 71, 781-791.	0.9	8
38	Totally self-checking checkers for Borden codes. International Journal of Electronics, 1994, 76, 57-64.	0.9	8
39	Efficient totally self-checking checkers for a class of Borden codes. IEEE Transactions on Computers, 1995, 44, 1318-1322.	2.4	8
40	Efficient field-programmable gate array implementation of CCSDS 121.0-B-2 lossless data compression algorithm for image compression. Journal of Applied Remote Sensing, 2015, 9, 097499.	0.6	8
41	Efficient PL A design of TSC 1-out-of- $n$ code checkers. International Journal of Electronics, 1992, 73, 471-484.	0.9	5
42	Efficient structured design of totally self-checking $M$ -out-of- $N$ code checkers with $M \geq 2$ and $N = 2^k - 1$ . International Journal of Electronics, 1994, 77, 251-257.	0.9	5
43	Testing CMOS combinational iterative logic arrays for realistic faults. The Integration VLSI Journal, 1996, 21, 209-228.	1.3	5
44	Software-Based Self-Testing of Embedded Processors. , 2007, , 447-481.		5
45	Recent achievements on ASPIICS, an externally occulted coronagraph for PROBA-3. Proceedings of SPIE, 2016, , .	0.8	5
46	Fast C-testable array multipliers. International Journal of Electronics, 1996, 80, 561-582.	0.9	4
47	Concurrent Delay Testing in Totally Self-Checking Systems. Journal of Electronic Testing: Theory and Applications (JETTA), 1998, 12, 55-61.	0.9	4
48	Testability Analysis and Scalable Test Generation for High-Speed Floating-Point Units. IEEE Transactions on Computers, 2006, 55, 1449-1457.	2.4	4
49	Online error detection in multiprocessor chips: A test scheduling study. , 2013, , .		4
50	Analyzing the Resilience to SEUs of an Image Data Compression Core in a COTS SRAM FPGA. , 2019, , .		4
51	Robust test generation for transistor stuck-open faults in CMOS complex gates. International Journal of Electronics, 1995, 79, 129-142.	0.9	3
52	An Effective Deterministic BIST Scheme for Shifter/Accumulator Pairs in Datapaths. Journal of Electronic Testing: Theory and Applications (JETTA), 2001, 17, 97-107.	0.9	3
53	Dependable reconfigurable space systems: Challenges, new trends and case studies. , 2014, , .		2
54	Efficient Hardware Architectures and Implementations of Packet-Level Erasure Coding Schemes for High Data Rate Reliable Satellite Communications. IEEE Transactions on Aerospace and Electronic Systems, 2022, 58, 2269-2280.	2.6	2

#	ARTICLE	IF	CITATIONS
55	Concurrently totally self-checking microprogram control unit with duplication of microprogram sequencer. <i>Microprocessing and Microprogramming</i> , 1987, 20, 271-281.	0.3	1
56	A single chip dependable and adaptable payload Data Processing Unit. , 2015, , .		1
57	Application-Specific Solutions. , 2018, , 189-216.		1
58	Hierarchical robust test generation for CMOS circuit stuck-open faults. <i>International Journal of Electronics</i> , 1997, 82, 45-60.	0.9	0
59	Testable designs of one-count generators. <i>International Journal of Electronics</i> , 1998, 85, 629-650.	0.9	0
60	On robust two-pattern testing of one-dimensional CMOS iterative logic arrays. <i>International Journal of Electronics</i> , 1999, 86, 967-978.	0.9	0