Ettore Napoli

List of Publications by Year
in descending order

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Version: 2024-02-01

76 papers	1,519 citations	361413 20 h-index	345221 36 g-index

77 all docs	77 docs citations	77 times ranked	847 citing authors

#	Article	IF	Citations
1	A Novel Module-Sign Low-Power Implementation for the DLMS Adaptive Filter With Low Steady-State Error. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 297-308.	5.4	6
2	Approximate Multipliers Using Static Segmentation: Error Analysis and Improvements. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 2449-2462.	5.4	19
3	Enabling Fine Sample Rate Settings in DSOs with Time-Interleaved ADCs. Sensors, 2022, 22, 234.	3.8	1
4	Approximate Recursive Multipliers Using Low Power Building Blocks. IEEE Transactions on Emerging Topics in Computing, 2022, 10, 1315-1330.	4.6	14
5	Approximate Recursive Multipliers Using Carry Truncation and Error Compensation. , 2022, , .		2
6	Real-Time Downsampling in Digital Storage Oscilloscopes With Multichannel Architectures. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 4142-4155.	5.4	4
7	A Time Base Option for Arbitrary Selection of Sample Rate in Digital Storage Oscilloscopes. IEEE Transactions on Instrumentation and Measurement, 2020, 69, 3936-3948.	4.7	8
8	A Binary Line Buffer Circuit Featuring Lossy Data Compression at Fixed Maximum Data Rate. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 121-134.	5.4	0
9	Low-Power Approximate Multiplier with Error Recovery using a New Approximate 4-2 Compressor. , 2020, , .		16
10	A 1.45 GHz All-Digital Spread Spectrum Clock Generator in 65nm CMOS for Synchronization-Free SoC Applications. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 3839-3852.	5.4	4
11	Comparison and Extension of Approximate 4-2 Compressors for Low-Power Approximate Multipliers. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 3021-3034.	5.4	141
12	Digital Circuit for Seamless Resampling ADC Output Streams. Sensors, 2020, 20, 1619.	3.8	11
13	Variable-Rounded LMS Filter for Low-Power Applications. Lecture Notes in Electrical Engineering, 2020, , 155-161.	0.4	1
14	Low-power Implementation of LMS Adaptive Filters Using Scalable Rounding. , 2020, , .		1
15	Low-Power Hardware Implementation of Least-Mean-Square Adaptive Filters Using Approximate Arithmetic. Circuits, Systems, and Signal Processing, 2019, 38, 5606-5622.	2.0	7
16	Design of Low-Power Approximate LMS Filters with Precision-Scalability. Lecture Notes in Electrical Engineering, 2019, , 237-243.	0.4	2
17	Quality-Scalable Approximate LMS Filter. , 2018, , .		6
18	A Standard-Cell-Based All-Digital PWM Modulator With High Resolution and Spread- Spectrum Capability. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 3885-3896.	5.4	18

#	Article	IF	Citations
19	On the Use of Approximate Multipliers in LMS Adaptive Filters. , 2018, , .		9
20	Approximate Multipliers Based on New Approximate Compressors. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 4169-4182.	5.4	171
21	Stall-Aware Fixed-Point Implementation of LMS Filters. , 2018, , .		1
22	A SISO Register Circuit Tailored for Input Data with Low Transition Probability. IEEE Transactions on Computers, 2017, 66, 45-51.	3.4	1
23	Single Bit Filtering Circuit Implemented in a System for the Generation of Colored Noise. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 1040-1050.	5.4	1
24	Single Flip-Flop Driving Circuit for Glitch-Free NAND-Based Digitally Controlled Delay-Lines. Circuits, Systems, and Signal Processing, 2017, 36, 1341-1360.	2.0	3
25	On the use of approximate adders in carry-save multiplier-accumulators. , 2017, , .		19
26	A 3.3 GHz Spread-Spectrum Clock Generator Supporting Discontinuous Frequency Modulations in 28 nm CMOS. IEEE Journal of Solid-State Circuits, 2015, 50, 2074-2089.	5.4	15
27	FPGA implementation of the CCSDS-123.0-B-1 lossless Hyperspectral Image compression algorithm prediction stage. , 2015, , .		4
28	An FPGA processor for real-time, fixed-point refinement of CDVS keypoints. , 2015, , .		0
29	Effect of the Collector Design on the IGBT Avalanche Ruggedness: A Comparative Analysis Between Punch-Through and Field-Stop Devices. IEEE Transactions on Electron Devices, 2015, 62, 2535-2541.	3.0	15
30	A Frequency Domain Processor for Real-Time CDVS Keypoints Extraction. , 2014, , .		0
31	High Speed Speculative Multipliers Based on Speculative Carry-Save Tree. IEEE Transactions on Circuits and Systems I: Regular Papers, 2014, 61, 3426-3435.	5.4	42
32	Analysis and comparison of Direct Digital Frequency Synthesizers implemented on FPGA. The Integration VLSI Journal, 2014, 47, 261-271.	2.1	13
33	Truncated squarer with minimum mean-square error. Microelectronics Journal, 2014, 45, 799-804.	2.0	10
34	Physics of the Negative Resistance in the Avalanche <inline-formula> <tex-math notation="TeX">$I{-}V$ </tex-math></inline-formula> Curve of Field Stop IGBTs: Collector Design Rules for Improved Ruggedness. IEEE Transactions on Electron Devices, 2014, 61, 1457-1463.	3.0	21
35	Impact of Donor Traps on the 2DEG and Electrical Behavior of AlGaN/GaN MISFETs. IEEE Electron Device Letters, 2014, 35, 27-29.	3.9	40
36	Design and Implementation of a Preprocessing Circuit for Bandpass Signals Acquisition. IEEE Transactions on Instrumentation and Measurement, 2014, 63, 287-294.	4.7	26

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37	Accurate Fixed-Point Logarithmic Converter. IEEE Transactions on Circuits and Systems II: Express Briefs, 2014, 61, 526-530.	3.0	20
38	Hardware performance versus video quality trade-off for Gaussian mixture model based background identification systems. , 2014, , .		2
39	FPGA-based architecture for real time segmentation and denoising of HD video. Journal of Real-Time Image Processing, 2013, 8, 389-401.	3.5	47
40	Fixed-Width Multipliers and Multipliers-Accumulators With Min-Max Approximation Error. IEEE Transactions on Circuits and Systems I: Regular Papers, 2013, 60, 2375-2388.	5.4	44
41	Direct Digital Frequency Synthesizers implemented on high end FPGA devices. , 2013, , .		3
42	FPGA Implementation of Gaussian Mixture Model Algorithm for 47â€‰fps Segmentation of 1080p Video. Journal of Electrical and Computer Engineering, 2013, 2013, 1-8.	0.9	8
43	Processor core for real time background identification of HD video based on OpenCV Gaussian mixture model algorithm. Proceedings of SPIE, 2013, , .	0.8	0
44	An FPGA-based Real-time Background Identification Circuit for 1080p Video. , 2012, , .		4
45	3D electro-thermal simulations of wide area power devices operating in avalanche condition. Microelectronics Reliability, 2012, 52, 2385-2390.	1.7	16
46	Design of Fixed-Width Multipliers With Linear Compensation Function. IEEE Transactions on Circuits and Systems I: Regular Papers, 2011, 58, 947-960.	5.4	57
47	Analytical Calculation of the Maximum Error for a Family of Truncated Multipliers Providing Minimum Mean Square Error. IEEE Transactions on Computers, 2011, 60, 1366-1371.	3.4	17
48	Analysis of large area Trench-IGBT current distribution under UIS test with the aid of lock-in thermography. Microelectronics Reliability, 2010, 50, 1725-1730.	1.7	27
49	A novel UIS test system with Crowbar feedback for reduced failure energy in power devices testing. Microelectronics Reliability, 2010, 50, 1479-1483.	1.7	7
50	High-speed differential resistor ladder for A/D converters. , 2010, , .		1
51	Truncated Binary Multipliers With Variable Correction and Minimum Mean Square Error. IEEE Transactions on Circuits and Systems I: Regular Papers, 2010, 57, 1312-1325.	5.4	96
52	On the static performance of the RESURF LDMOSFETS for power ICs. Power Semiconductor Devices & IC's, 2009 ISPSD 2009 21st International Symposium on, 2009, , .	0.0	77
53	Breakdown Voltage for Superjunction Power Devices With Charge Imbalance: An Analytical Model Valid for Both Punch Through and Non Punch Through Devices. IEEE Transactions on Electron Devices, 2009, 56, 3175-3183.	3.0	57
54	1300V, 2ms pulse inductive load switching test circuit with 20ns selectable crowbar intervention. Microelectronics Reliability, 2009, 49, 1386-1390.	1.7	9

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55	Detection of localized UIS failure on IGBTs with the aid of lock-in thermography. Microelectronics Reliability, 2008, 48, 1432-1434.	1.7	25
56	The Effect of Charge Imbalance on Superjunction Power Devices: An Exact Analytical Solution. IEEE Electron Device Letters, 2008, 29, 249-251.	3.9	42
57	Constrained piecewise polinomial approximation for hardware implementation of elementary functions. , 2008, , .		2
58	Duration of the High Breakdown Voltage Phase in Deep Depletion SOI LDMOS. IEEE Electron Device Letters, 2007, 28, 753-755.	3.9	8
59	Study of a failure mechanism during UIS switching of planar PT-IGBT with current sense cell. Microelectronics Reliability, 2007, 47, 1756-1760.	1.7	11
60	Limits and application of the newly proposed deep-depletion SOI LDMOS. IET Circuits, Devices and Systems, 2007, 1, 366.	1.4	2
61	Substrate engineering for improved transient breakdown voltage in SOI lateral power MOS. IEEE Electron Device Letters, 2006, 27, 678-680.	3.9	7
62	An Analytical Model for the Lateral Insulated Gate Bipolar Transistor (LIGBT) on Thin SOI. IEEE Transactions on Power Electronics, 2006, 21, 1521-1528.	7.9	11
63	Modeling turn-off voltage rise in SOI LIGBT. Journal of Computational Electronics, 2006, 5, 181-186.	2.5	1
64	Modeling Voltage Derivative During Inductive Turnoff in Thin SOI LIGBT. IEEE Transactions on Electron Devices, 2005, 52, 2776-2783.	3.0	9
65	A Complete Isothermal Model for the Lateral Insulated Gate Bipolar Transistor on SOI technology. , 2005, , .		2
66	Design of IGBT with integral freewheeling diode. IEEE Electron Device Letters, 2002, 23, 532-534.	3.9	27
67	Low-power flip-flops with reliable clock gating. Microelectronics Journal, 2001, 32, 21-28.	2.0	16
68	Power superjunction devices: an analytic model for breakdown voltage. Microelectronics Journal, 2001, 32, 491-496.	2.0	22
69	Optimal ON-resistance versus breakdown voltage tradeoff in superjunction power devices: a novel analytical model. IEEE Transactions on Electron Devices, 2001, 48, 2161-2167.	3.0	67
70	Analysis of power dissipation in double edge-triggered flip-flops. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2000, 8, 624-629.	3.1	38
71	Bidimensional lifetime control for high-speed low-loss p-i-n rectifiers. IEEE Transactions on Power Electronics, 2000, 15, 791-798.	7.9	8
72	Fast power rectifier design using local lifetime and emitter efficiency control techniques. Microelectronics Journal, 1999, 30, 505-512.	2.0	11

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73	Numerical analysis of local lifetime control for high-speed low-loss P-i-N diode design. IEEE Transactions on Power Electronics, 1999, 14, 615-621.	7.9	33
74	Low power double edge-triggered flip-flop using one latch. Electronics Letters, 1999, 35, 187.	1.0	20
75	Power rectifier model including self heating effects. Microelectronics Reliability, 1998, 38, 1899-1906.	1.7	9
76	Performance analysis of a two-level carry-skip adder implemented in complementary pass-transistor logic. Microelectronics Journal, 1998, 29, 755-760.	2.0	0