Puneet Gupta

List of Publications by Year in Descending Order

146 papers	1,672 citations	17 h-index	34 g-index
186 ext. papers	2,262 ext. citations	2.4 avg, IF	4.93 L-index

#	Paper	IF	Citations
146	DRDebug: Automated Design Rule Debugging. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2022**, 1-1	2.5	
145	Lightweight Software-Defined Error Correction for Memories. *Embedded Systems*, **2021**, 207-232		0
144	Adaptive MRAM Write and Read with MTJ Variation Monitor. *IEEE Transactions on Emerging Topics in Computing*, **2021**, 9, 402-413	4.1	5
143	Reverse Engineering for 2.5-D Split Manufactured ICs. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2020**, 39, 3128-3133	2.5	3
142	Design Space Exploration for Chiplet-Assembly-Based Processors. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2020**, 28, 1062-1073	2.6	2
141	Massively parallel amplitude-only Fourier neural network. *Optica*, **2020**, 7, 1812	8.6	20
140	Million-channel parallelism Fourier-optic convolutional filter and neural network processor **2020**,		1
139	3PXNet. *Transactions on Embedded Computing Systems*, **2020**, 19, 1-23	1.8	3
138	Design Impacts of Back-End-of-Line Line Edge Roughness. *IEEE Transactions on Semiconductor Manufacturing*, **2020**, 33, 32-41	2.6	
137	ACOUSTIC: Accelerating Convolutional Neural Networks through Or-Unipolar Skipped Stochastic Computing **2020**,		3
136	. *IEEE Transactions on Information Forensics and Security*, **2020**, 15, 276-285	8	3
135	Architecting Waferscale Processors - A GPU Case Study **2019**,		6
134	Variability Expeditions: A Retrospective. *IEEE Design and Test*, **2019**, 36, 65-67	1.4	2
133	Context-Aware Resiliency: Unequal Message Protection for Random-Access Memories. *IEEE Transactions on Information Theory*, **2019**, 65, 6146-6159	2.8	2
132	Optimizing Multi-GPU Parallelization Strategies for Deep Learning Training. *IEEE Micro*, **2019**, 39, 91-101	1.8	19
131	Compression with multi-ECC **2019**,		3
130	Can the compressive strength of concrete be estimated from knowledge of the mixture proportions?: New insights from statistical analysis and machine learning methods. *Cement and Concrete Research*, **2019**, 115, 379-388	10.3	93

129	Analysis and Compact Modeling of Magnetic Tunnel Junctions Utilizing Voltage-Controlled Magnetic Anisotropy. *IEEE Transactions on Magnetics*, **2018**, 54, 1-9	2	16
128	Design and Analysis of Stability-Guaranteed PUFs. *IEEE Transactions on Information Forensics and Security*, **2018**, 13, 978-992	8	17
127	A Case for Packageless Processors **2018**,		6
126	Parity++: Lightweight Error Correction for Last Level Caches **2018**,		4
125	Assessing Layout Density Benefits of Vertical Channel Devices. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2018**, 37, 3211-3215	2.5	1
124	Dynamic programming approach to adaptive slicing for optimization under a global volumetric error constraint **2018**,		1
123	Defect avoidance for extreme ultraviolet mask defects using intentional pattern deformation **2018**,		1
122	Relaxing LER requirement in EUV lithography **2018**,		2
121	Assessing Benefits of a Buried Interconnect Layer in Digital Designs. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2017**, 36, 346-350	2.5	4
120	Benchmarking of Mask Fracturing Heuristics. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2017**, 36, 170-183	2.5	1
119	A Word Line Pulse Circuit Technique for Reliable Magnetoelectric Random Access Memory. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2017**, 25, 2027-2034	2.6	11
118	Write Error Rate and Read Disturbance in Electric-Field-Controlled Magnetic Random-Access Memory. *IEEE Magnetics Letters*, **2017**, 8, 1-5	1.6	22
117	Hybrid VC-MTJ/CMOS non-volatile stochastic logic for efficient computing **2017**,		7
116	Technology path-finding framework for directed-self assembly for via layers. *Journal of Micro/Nanolithography, MEMS, and MOEMS*, **2017**, 16, 013505	0.7	0
115	Tunneling Negative Differential Resistance-Assisted STT-RAM for Efficient Read and Write Operations. *IEEE Transactions on Electron Devices*, **2017**, 64, 121-129	2.9	14
114	Low-Cost Memory Fault Tolerance for IoT Devices. *Transactions on Embedded Computing Systems*, **2017**, 16, 1-25	1.8	7
113	System-Level Dynamic Variation Margining in Presence of Monitoring and Actuation. *IEEE Embedded Systems Letters*, **2017**, 9, 85-88	1	
112	Mask Assignment and DSA Grouping for DSA-MP Hybrid Lithography for Sub-7 nm Contact/Via Holes. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2017**, 36, 913-926	2.5	3

111	. *IEEE Computer Architecture Letters*, **2017**, 16, 51-55	1.8	8
110	Leveraging nMOS Negative Differential Resistance for Low Power, High Reliability Magnetic Memory. *IEEE Transactions on Electron Devices*, **2017**, 64, 4084-4090	2.9	3
109	**2017**,		13
108	Context-aware resiliency: Unequal message protection for random-access memories **2017**,		4
107	PROCEED: A Pareto Optimization-Based Circuit-Level Evaluator for Emerging Devices. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2016**, 24, 192-205	2.6	6
106	MTJ variation monitor-assisted adaptive MRAM write **2016**,		12
105	Source Line Sensing in Magneto-Electric Random-Access Memory to Reduce Read Disturbance and Improve Sensing Margin. *IEEE Magnetics Letters*, **2016**, 7, 1-5	1.6	10
104	X-Mem: A cross-platform and extensible memory characterization tool for the cloud **2016**,		7
103	Efficient Layout Generation and Design Evaluation of Vertical Channel Devices. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2016**, 35, 1449-1460	2.5	4
102	Multi-story power distribution networks for GPUs **2016**,		6
101	LEDPUF: Stability-guaranteed physical unclonable functions through locally enhanced defectivity **2016**,		6
100	An Evaluation Framework for Nanotransfer Printing-Based Feature-Level Heterogeneous Integration in VLSI Circuits. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2016**, 24, 1858-1870	2.6	2
99	Comparative Evaluation of Spin-Transfer-Torque and Magnetoelectric Random Access Memory. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, **2016**, 6, 134-145	5.2	58
98	MEMRES: A Fast Memory System Reliability Simulator. *IEEE Transactions on Reliability*, **2016**, 65, 1783-1797	4.6	6
97	Software-Defined Error-Correcting Codes **2016**,		8
96	Incorporating DSA in multipatterning semiconductor manufacturing technologies **2015**,		4
95	ViPZonE: Hardware Power Variability-Aware Virtual Memory Management for Energy Savings. *IEEE Transactions on Computers*, **2015**, 64, 1483-1496	2.5	6
94	Mask assignment and synthesis of DSA-MP hybrid lithography for sub-7nm contacts/vias **2015**,		29

93	NSF expedition on variability-aware software: Recent results and contributions. *IT - Information Technology*, **2015**, 57, 181-198	0.4	8
92	DPCS. *Transactions on Architecture and Code Optimization*, **2015**, 12, 1-26	1.3	9
91	Statistical timing and power analysis of VLSI considering non-linear dependence. *The Integration VLSI Journal*, **2014**, 47, 487-498	1.4	3
90	Synthesis and Analysis of Design-Dependent Ring Oscillator (DDRO) Performance Monitors. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2014**, 22, 2117-2130	2.6	12
89	PROCEED: A pareto optimization-based circuit-level evaluator for emerging devices **2014**,		6
88	EUV-CDA: Pattern shift aware critical density analysis for EUV mask layouts **2014**,		1
87	Comprehensive die-level assessment of design rules and layouts **2014**,		6
86	. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, **2014**, 4, 180-189	5.2	4
85	Multi-Layer Memory Resiliency **2014**,		10
84	Layout pattern-driven design rule evaluation **2014**,		1
83	Efficient layout generation and evaluation of vertical channel devices **2014**,		5
82	SlackProbe: A Flexible and Efficient In Situ Timing Slack Monitoring Methodology. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2014**, 33, 1168-1179	2.5	22
81	Comprehensive defect avoidance framework for mitigating EUV mask defects **2014**,		5
80	Benchmarking of mask fracturing heuristics **2014**,		2
79	Power / Capacity Scaling **2014**,		18
78	Accurate and inexpensive performance monitoring for variability-aware systems **2014**,		5
77	Layout pattern-driven design rule evaluation. *Journal of Micro/ Nanolithography, MEMS, and MOEMS* , **2014**, 13, 043018	0.7	5
76	Comprehensive defect avoidance framework for mitigating extreme ultraviolet mask defects. *Journal of Micro/ Nanolithography, MEMS, and MOEMS*, **2014**, 13, 043005	0.7	4

75	Reliable on-chip systems in the nano-era **2013**,		111
74	. *IEEE Transactions on Electron Devices*, **2013**, 60, 2186-2193	2.9	21
73	Framework for exploring the interaction between design rules and overlay control. *Journal of Micro/ Nanolithography, MEMS, and MOEMS*, **2013**, 12, 033014	0.7	2
72	Hardware Variability-Aware Duty Cycling for Embedded Sensors. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2013**, 21, 1000-1012	2.6	12
71	Design-Aware Defect-Avoidance Floorplanning of EUV Masks. *IEEE Transactions on Semiconductor Manufacturing*, **2013**, 26, 111-124	2.6	8
70	**2013**,		19
69	VarEMU: An emulation testbed for variability-aware software **2013**,		12
68	**2013**,		14
67	Variability-aware memory management for nanoscale computing **2013**,		3
66	Towards analyzing and improving robustness of software applications to intermittent and permanent faults in hardware **2013**,		3
65	Underdesigned and Opportunistic Computing in Presence of Hardware Variability. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2013**, 32, 8-23	2.5	88
64	A framework for exploring the interaction between design rules and overlay control **2013**,		4
63	Discrete sizing for leakage power optimization in physical design. *ACM Transactions on Design Automation of Electronic Systems*, **2013**, 18, 1-11	1.5	2
62	ECO cost measurement and incremental gate sizing for late process changes. *ACM Transactions on Design Automation of Electronic Systems*, **2013**, 18, 1-11	1.5	3
61	. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2013**, 32, 202-215	2.5	16
60	Role of design in multiple patterning: Technology development, design enablement and process control **2013**,		2
59	Design-Aware Mask Inspection. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2012**, 31, 690-702	2.5	3
58	. *IEEE Transactions on Electron Devices*, **2012**, 59, 2057-2063	2.9	32

57	Power Variability in Contemporary DRAMs. *IEEE Embedded Systems Letters*, **2012**, 4, 37-40	1	11
56	Design-Dependent Process Monitoring for Wafer Manufacturing and Test Cost Reduction. *IEEE Transactions on Semiconductor Manufacturing*, **2012**, 25, 447-459	2.6	1
55	AppAdapt: Opportunistic Application Adaptation in Presence of Hardware Variation. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2012**, 20, 1986-1996	2.6	10
54	Discrete Circuit Optimization. *Foundations and Trends in Electronic Design Automation*, **2012**, 6, 1-120	1	2
53	A methodology for the early exploration of design rules for multiple-patterning technologies **2012**,		5
52	ViPZonE **2012**,		13
51	DRE: A Framework for Early Co-Evaluation of Design Rules, Technology Choices, and Layout Methodologies. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2012** , 31, 1379-1392	2.5	12
50	VaMV: Variability-aware Memory Virtualization **2012**,		8
49	DDRO: A novel performance monitoring methodology based on design-dependent ring oscillators **2012**,		15
48	A novel methodology for triple/multiple-patterning layout decomposition **2012**,		8
47	Defect-aware reticle floorplanning for EUV masks **2011**,		6
46	. *IEEE Transactions on Semiconductor Manufacturing*, **2011**, 24, 93-103	2.6	11
45	Physically Justifiable Die-Level Modeling of Spatial Variation in View of Systematic Across Wafer Variability. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2011**, 30, 388-401	2.5	21
44	**2011**,		5
43	Variability-aware duty cycle scheduling in long running embedded sensing systems **2011**,		9
42	Trading Accuracy for Power with an Underdesigned Multiplier Architecture **2011**,		238
41	Underdesigned and Opportunistic Computing **2011**,		1
40	Trading Accuracy for Power in a Multiplier Architecture. *Journal of Low Power Electronics*, **2011**, 7, 490-501	1.2	67

39	Incremental gate sizing for late process changes **2010**,		5
38	Design dependent process monitoring for back-end manufacturing cost reduction **2010**,		10
37	Design-aware mask inspection **2010**,		2
36	Electrical Modeling of Lithographic Imperfections **2010**,		11
35	Evaluating Statistical Power Optimization. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2010**, 29, 1750-1762	2.5	3
34	Variation-aware speed binning of multi-core processors **2010**,		12
33	On Electrical Modeling of Imperfect Diffusion Patterning **2010**,		3
32	What is process window?. *ACM SIGDA Newsletter*, **2010**, 40, 1-1		5
31	Eyecharts **2010**,		10
30	Software adaptation in quality sensitive applications to deal with hardware variability **2010**,		10
29	Accounting for non-linear dependence using function driven component analysis **2009**,		4
28	Physically justifiable die-level modeling of spatial variation in view of systematic across wafer variability **2009**,		12
27	On the futility of statistical power optimization **2009**,		1
26	Efficient Additive Statistical Leakage Estimation. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2009**, 28, 1777-1781	2.5	9
25	Design-overlay interactions in metal double patterning **2009**,		6
24	A framework for early and systematic evaluation of design rules **2009**,		8
23	Investigation of diffusion rounding for post-lithography analysis **2008**,		6
22	Electrical metrics for lithographic line-end tapering **2008**,		5

21	Shaping gate channels for improved devices **2008**,		2
20	Self-Compensating Design for Reduction of Timing and Leakage Sensitivity to Systematic Pattern-Dependent Variation. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2007**, 26, 1614-1624	2.5	2
19	Lithography simulation-based full-chip design analyses **2006**,		8
18	Modeling of non-uniform device geometries for post-lithography circuit analysis **2006**,		11
17	Wafer Topography-Aware Optical Proximity Correction. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2006**, 25, 2747-2756	2.5	14
16	Modeling edge placement error distribution in standard cell library **2006**, 6156, 265		4
15	Toward through-process layout quality metrics **2005**,		8
14	Manufacturing-aware design methodology for assist feature correctness **2005**,		2
13	Wafer topography-aware optical proximity correction for better DOF margin and CD control **2005**,		5
12	Interaction and balance of mask write time and design RET strategies **2005**,		2
11	Improving OPC quality via interactions within the design-to-manufacturing flow (Invited Paper) **2005**, 5853, 131		
10	Modeling OPC complexity for design for manufacturability **2005**, 5992, 612		3
9	Quantifying Error in Dynamic Power Estimation of CMOS Circuits. *Analog Integrated Circuits and Signal Processing*, **2005**, 42, 253-264	1.2	2
8	Routing-aware scan chain ordering. *ACM Transactions on Design Automation of Electronic Systems*, **2005**, 10, 546-560	1.5	6
7	Detailed placement for improved depth of focus and CD control **2005**,		10
6	Selective gate-length biasing for cost-effective runtime leakage control **2004**,		11
5	Investigation of performance metrics for interconnect stack architectures **2004**,		4
4	Toward a systematic-variation aware timing methodology **2004**,		10

3	Merits of cellwise model-based OPC **2004**,	10
2	Performance-impact limited area fill synthesis **2003**,	25
1	Performance-impact limited-area fill synthesis **2003**,	2