

Puneet Gupta

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The third column is the impact factor (IF) of the journal, and the fourth column is the number of citations of the article.

146
papers

1,672
citations

17
h-index

34
g-index

186
ext. papers

2,262
ext. citations

2.4
avg, IF

4.93
L-index

#	Paper	IF	Citations
146	Trading Accuracy for Power with an Underdesigned Multiplier Architecture 2011 ,		238
145	Reliable on-chip systems in the nano-era 2013 ,		111
144	Can the compressive strength of concrete be estimated from knowledge of the mixture proportions?: New insights from statistical analysis and machine learning methods. <i>Cement and Concrete Research</i> , 2019 , 115, 379-388	10.3	93
143	Underdesigned and Opportunistic Computing in Presence of Hardware Variability. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2013 , 32, 8-23	2.5	88
142	Trading Accuracy for Power in a Multiplier Architecture. <i>Journal of Low Power Electronics</i> , 2011 , 7, 490-501		67
141	Comparative Evaluation of Spin-Transfer-Torque and Magnetoelectric Random Access Memory. <i>IEEE Journal on Emerging and Selected Topics in Circuits and Systems</i> , 2016 , 6, 134-145	5.2	58
140	. <i>IEEE Transactions on Electron Devices</i> , 2012 , 59, 2057-2063	2.9	32
139	Mask assignment and synthesis of DSA-MP hybrid lithography for sub-7nm contacts/vias 2015 ,		29
138	Performance-impact limited area fill synthesis 2003 ,		25
137	Write Error Rate and Read Disturbance in Electric-Field-Controlled Magnetic Random-Access Memory. <i>IEEE Magnetism Letters</i> , 2017 , 8, 1-5	1.6	22
136	SlackProbe: A Flexible and Efficient In Situ Timing Slack Monitoring Methodology. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2014 , 33, 1168-1179	2.5	22
135	. <i>IEEE Transactions on Electron Devices</i> , 2013 , 60, 2186-2193	2.9	21
134	Physically Justifiable Die-Level Modeling of Spatial Variation in View of Systematic Across Wafer Variability. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2011 , 30, 388-401	2.5	21
133	Massively parallel amplitude-only Fourier neural network. <i>Optica</i> , 2020 , 7, 1812	8.6	20
132	Optimizing Multi-GPU Parallelization Strategies for Deep Learning Training. <i>IEEE Micro</i> , 2019 , 39, 91-101	1.8	19
131	2013 ,		19
130	Power / Capacity Scaling 2014 ,		18

129	Design and Analysis of Stability-Guaranteed PUFs. <i>IEEE Transactions on Information Forensics and Security</i> , 2018 , 13, 978-992	8	17
128	Analysis and Compact Modeling of Magnetic Tunnel Junctions Utilizing Voltage-Controlled Magnetic Anisotropy. <i>IEEE Transactions on Magnetics</i> , 2018 , 54, 1-9	2	16
127	. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2013 , 32, 202-215	2.5	16
126	DDRO: A novel performance monitoring methodology based on design-dependent ring oscillators 2012 ,		15
125	Tunneling Negative Differential Resistance-Assisted STT-RAM for Efficient Read and Write Operations. <i>IEEE Transactions on Electron Devices</i> , 2017 , 64, 121-129	2.9	14
124	2013 ,		14
123	Wafer Topography-Aware Optical Proximity Correction. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2006 , 25, 2747-2756	2.5	14
122	2017 ,		13
121	VipZone 2012 ,		13
120	MTJ variation monitor-assisted adaptive MRAM write 2016 ,		12
119	Synthesis and Analysis of Design-Dependent Ring Oscillator (DDRO) Performance Monitors. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , 2014 , 22, 2117-2130	2.6	12
118	Hardware Variability-Aware Duty Cycling for Embedded Sensors. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , 2013 , 21, 1000-1012	2.6	12
117	VarEMU: An emulation testbed for variability-aware software 2013 ,		12
116	Variation-aware speed binning of multi-core processors 2010 ,		12
115	Physically justifiable die-level modeling of spatial variation in view of systematic across wafer variability 2009 ,		12
114	DRE: A Framework for Early Co-Evaluation of Design Rules, Technology Choices, and Layout Methodologies. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2012 , 31, 1379-1392	2.5	12
113	A Word Line Pulse Circuit Technique for Reliable Magnetoelectric Random Access Memory. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , 2017 , 25, 2027-2034	2.6	11
112	Power Variability in Contemporary DRAMs. <i>IEEE Embedded Systems Letters</i> , 2012 , 4, 37-40	1	11

111	. <i>IEEE Transactions on Semiconductor Manufacturing</i> , 2011 , 24, 93-103	2.6	11
110	Electrical Modeling of Lithographic Imperfections 2010 ,		11
109	Modeling of non-uniform device geometries for post-lithography circuit analysis 2006 ,		11
108	Selective gate-length biasing for cost-effective runtime leakage control 2004 ,		11
107	Source Line Sensing in Magneto-Electric Random-Access Memory to Reduce Read Disturbance and Improve Sensing Margin. <i>IEEE Magnetics Letters</i> , 2016 , 7, 1-5	1.6	10
106	Multi-Layer Memory Resiliency 2014 ,		10
105	AppAdapt: Opportunistic Application Adaptation in Presence of Hardware Variation. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , 2012 , 20, 1986-1996	2.6	10
104	Design dependent process monitoring for back-end manufacturing cost reduction 2010 ,		10
103	Eyecharts 2010 ,		10
102	Toward a systematic-variation aware timing methodology 2004 ,		10
101	Merits of cellwise model-based OPC 2004 ,		10
100	Detailed placement for improved depth of focus and CD control 2005 ,		10
99	Software adaptation in quality sensitive applications to deal with hardware variability 2010 ,		10
98	Variability-aware duty cycle scheduling in long running embedded sensing systems 2011 ,		9
97	Efficient Additive Statistical Leakage Estimation. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2009 , 28, 1777-1781	2.5	9
96	DPCS. <i>Transactions on Architecture and Code Optimization</i> , 2015 , 12, 1-26	1.3	9
95	Design-Aware Defect-Avoidance Floorplanning of EUV Masks. <i>IEEE Transactions on Semiconductor Manufacturing</i> , 2013 , 26, 111-124	2.6	8
94	. <i>IEEE Computer Architecture Letters</i> , 2017 , 16, 51-55	1.8	8

93	NSF expedition on variability-aware software: Recent results and contributions. <i>IT - Information Technology</i> , 2015 , 57, 181-198	0.4	8
92	VaMV: Variability-aware Memory Virtualization 2012 ,		8
91	A novel methodology for triple/multiple-patterning layout decomposition 2012 ,		8
90	Lithography simulation-based full-chip design analyses 2006 ,		8
89	Toward through-process layout quality metrics 2005 ,		8
88	A framework for early and systematic evaluation of design rules 2009 ,		8
87	Software-Defined Error-Correcting Codes 2016 ,		8
86	Hybrid VC-MTJ/CMOS non-volatile stochastic logic for efficient computing 2017 ,		7
85	Low-Cost Memory Fault Tolerance for IoT Devices. <i>Transactions on Embedded Computing Systems</i> , 2017 , 16, 1-25	1.8	7
84	X-Mem: A cross-platform and extensible memory characterization tool for the cloud 2016 ,		7
83	PROCEED: A Pareto Optimization-Based Circuit-Level Evaluator for Emerging Devices. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , 2016 , 24, 192-205	2.6	6
82	Architecting Waferscale Processors - A GPU Case Study 2019 ,		6
81	ViPZone: Hardware Power Variability-Aware Virtual Memory Management for Energy Savings. <i>IEEE Transactions on Computers</i> , 2015 , 64, 1483-1496	2.5	6
80	A Case for Packageless Processors 2018 ,		6
79	PROCEED: A pareto optimization-based circuit-level evaluator for emerging devices 2014 ,		6
78	Comprehensive die-level assessment of design rules and layouts 2014 ,		6
77	Defect-aware reticle floorplanning for EUV masks 2011 ,		6
76	Design-overlay interactions in metal double patterning 2009 ,		6

75	Investigation of diffusion rounding for post-lithography analysis 2008,		6
74	Routing-aware scan chain ordering. <i>ACM Transactions on Design Automation of Electronic Systems</i> , 2005 , 10, 546-560	1.5	6
73	Multi-story power distribution networks for GPUs 2016,		6
72	LEDPUF: Stability-guaranteed physical unclonable functions through locally enhanced defectivity 2016,		6
71	MEMRES: A Fast Memory System Reliability Simulator. <i>IEEE Transactions on Reliability</i> , 2016 , 65, 1783-1797	1.7	6
70	Efficient layout generation and evaluation of vertical channel devices 2014,		5
69	Comprehensive defect avoidance framework for mitigating EUV mask defects 2014,		5
68	Accurate and inexpensive performance monitoring for variability-aware systems 2014,		5
67	Layout pattern-driven design rule evaluation. <i>Journal of Micro/Nanolithography, MEMS, and MOEMS</i> , 2014 , 13, 043018	0.7	5
66	Incremental gate sizing for late process changes 2010,		5
65	2011,		5
64	A methodology for the early exploration of design rules for multiple-patterning technologies 2012,		5
63	What is process window?. <i>ACM SIGDA Newsletter</i> , 2010 , 40, 1-1		5
62	Electrical metrics for lithographic line-end tapering 2008,		5
61	Wafer topography-aware optical proximity correction for better DOF margin and CD control 2005,		5
60	Adaptive MRAM Write and Read with MTJ Variation Monitor. <i>IEEE Transactions on Emerging Topics in Computing</i> , 2021 , 9, 402-413	4.1	5
59	Assessing Benefits of a Buried Interconnect Layer in Digital Designs. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2017 , 36, 346-350	2.5	4
58	Incorporating DSA in multipatterning semiconductor manufacturing technologies 2015,		4

57	Efficient Layout Generation and Design Evaluation of Vertical Channel Devices. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2016 , 35, 1449-1460	2.5	4
56	Parity++: Lightweight Error Correction for Last Level Caches 2018 ,		4
55	. <i>IEEE Journal on Emerging and Selected Topics in Circuits and Systems</i> , 2014 , 4, 180-189	5.2	4
54	Context-aware resiliency: Unequal message protection for random-access memories 2017 ,		4
53	Comprehensive defect avoidance framework for mitigating extreme ultraviolet mask defects. <i>Journal of Micro/ Nanolithography, MEMS, and MOEMS</i> , 2014 , 13, 043005	0.7	4
52	A framework for exploring the interaction between design rules and overlay control 2013 ,		4
51	Accounting for non-linear dependence using function driven component analysis 2009 ,		4
50	Modeling edge placement error distribution in standard cell library 2006 , 6156, 265		4
49	Investigation of performance metrics for interconnect stack architectures 2004 ,		4
48	Reverse Engineering for 2.5-D Split Manufactured ICs. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2020 , 39, 3128-3133	2.5	3
47	Statistical timing and power analysis of VLSI considering non-linear dependence. <i>The Integration VLSI Journal</i> , 2014 , 47, 487-498	1.4	3
46	Design-Aware Mask Inspection. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2012 , 31, 690-702	2.5	3
45	Variability-aware memory management for nanoscale computing 2013 ,		3
44	Towards analyzing and improving robustness of software applications to intermittent and permanent faults in hardware 2013 ,		3
43	Mask Assignment and DSA Grouping for DSA-MP Hybrid Lithography for Sub-7 nm Contact/Via Holes. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2017 , 36, 913-926	2.5	3
42	Leveraging nMOS Negative Differential Resistance for Low Power, High Reliability Magnetic Memory. <i>IEEE Transactions on Electron Devices</i> , 2017 , 64, 4084-4090	2.9	3
41	ECO cost measurement and incremental gate sizing for late process changes. <i>ACM Transactions on Design Automation of Electronic Systems</i> , 2013 , 18, 1-11	1.5	3
40	Evaluating Statistical Power Optimization. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2010 , 29, 1750-1762	2.5	3

39	On Electrical Modeling of Imperfect Diffusion Patterning 2010 ,		3
38	Modeling OPC complexity for design for manufacturability 2005 , 5992, 612		3
37	3PXNet. <i>Transactions on Embedded Computing Systems</i> , 2020 , 19, 1-23	1.8	3
36	Compression with multi-ECC 2019 ,		3
35	ACOUSTIC: Accelerating Convolutional Neural Networks through Or-Unipolar Skipped Stochastic Computing 2020 ,		3
34	. <i>IEEE Transactions on Information Forensics and Security</i> , 2020 , 15, 276-285	8	3
33	Variability Expeditions: A Retrospective. <i>IEEE Design and Test</i> , 2019 , 36, 65-67	1.4	2
32	Design Space Exploration for Chiplet-Assembly-Based Processors. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , 2020 , 28, 1062-1073	2.6	2
31	Context-Aware Resiliency: Unequal Message Protection for Random-Access Memories. <i>IEEE Transactions on Information Theory</i> , 2019 , 65, 6146-6159	2.8	2
30	Framework for exploring the interaction between design rules and overlay control. <i>Journal of Micro/ Nanolithography, MEMS, and MOEMS</i> , 2013 , 12, 033014	0.7	2
29	Benchmarking of mask fracturing heuristics 2014 ,		2
28	Discrete Circuit Optimization. <i>Foundations and Trends in Electronic Design Automation</i> , 2012 , 6, 1-120	1	2
27	Discrete sizing for leakage power optimization in physical design. <i>ACM Transactions on Design Automation of Electronic Systems</i> , 2013 , 18, 1-11	1.5	2
26	Role of design in multiple patterning: Technology development, design enablement and process control 2013 ,		2
25	Design-aware mask inspection 2010 ,		2
24	Shaping gate channels for improved devices 2008 ,		2
23	Self-Compensating Design for Reduction of Timing and Leakage Sensitivity to Systematic Pattern-Dependent Variation. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2007 , 26, 1614-1624	2.5	2
22	Manufacturing-aware design methodology for assist feature correctness 2005 ,		2

21	Interaction and balance of mask write time and design RET strategies 2005 ,		2
20	Quantifying Error in Dynamic Power Estimation of CMOS Circuits. <i>Analog Integrated Circuits and Signal Processing</i> , 2005 , 42, 253-264	1.2	2
19	Performance-impact limited-area fill synthesis 2003 ,		2
18	Relaxing LER requirement in EUV lithography 2018 ,		2
17	An Evaluation Framework for Nanotransfer Printing-Based Feature-Level Heterogeneous Integration in VLSI Circuits. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , 2016 , 24, 1858-1870	2.6	2
16	Benchmarking of Mask Fracturing Heuristics. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2017 , 36, 170-183	2.5	1
15	Assessing Layout Density Benefits of Vertical Channel Devices. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2018 , 37, 3211-3215	2.5	1
14	EUV-CDA: Pattern shift aware critical density analysis for EUV mask layouts 2014 ,		1
13	Layout pattern-driven design rule evaluation 2014 ,		1
12	Design-Dependent Process Monitoring for Wafer Manufacturing and Test Cost Reduction. <i>IEEE Transactions on Semiconductor Manufacturing</i> , 2012 , 25, 447-459	2.6	1
11	Underdesigned and Opportunistic Computing 2011 ,		1
10	On the futility of statistical power optimization 2009 ,		1
9	Dynamic programming approach to adaptive slicing for optimization under a global volumetric error constraint 2018 ,		1
8	Defect avoidance for extreme ultraviolet mask defects using intentional pattern deformation 2018 ,		1
7	Million-channel parallelism Fourier-optic convolutional filter and neural network processor 2020 ,		1
6	Technology path-finding framework for directed-self assembly for via layers. <i>Journal of Micro/Nanolithography, MEMS, and MOEMS</i> , 2017 , 16, 013505	0.7	0
5	Lightweight Software-Defined Error Correction for Memories. <i>Embedded Systems</i> , 2021 , 207-232		0
4	System-Level Dynamic Variation Margining in Presence of Monitoring and Actuation. <i>IEEE Embedded Systems Letters</i> , 2017 , 9, 85-88	1	

- 3 Improving OPC quality via interactions within the design-to-manufacturing flow (Invited Paper)
2005, 5853, 131
- 2 Design Impacts of Back-End-of-Line Line Edge Roughness. *IEEE Transactions on Semiconductor Manufacturing*, **2020**, 33, 32-41 2.6
- 1 DRDebug: Automated Design Rule Debugging. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2022**, 1-1 2.5