Puneet Gupta

List of Publications by Year in descending order

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185 papers	2,836 citations	471371 17 h-index	377752 34 g-index
186 all docs	186 docs citations	186 times ranked	1825 citing authors

#	Article	IF	Citations
1	Trading Accuracy for Power with an Underdesigned Multiplier Architecture. , 2011, , .		363
2	Can the compressive strength of concrete be estimated from knowledge of the mixture proportions?: New insights from statistical analysis and machine learning methods. Cement and Concrete Research, 2019, 115, 379-388.	4.6	207
3	Reliable on-chip systems in the nano-era. , 2013, , .		156
4	Underdesigned and Opportunistic Computing in Presence of Hardware Variability. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2013, 32, 8-23.	1.9	125
5	Massively parallel amplitude-only Fourier neural network. Optica, 2020, 7, 1812.	4.8	117
6	Trading Accuracy for Power in a Multiplier Architecture. Journal of Low Power Electronics, 2011, 7, 490-501.	0.6	91
7	Comparative Evaluation of Spin-Transfer-Torque and Magnetoelectric Random Access Memory. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2016, 6, 134-145.	2.7	81
8	Selective gate-length biasing for cost-effective runtime leakage control. , 2004, , .		44
9	Device- and Circuit-Level Variability Caused by Line Edge Roughness for Sub-32-nm FinFET Technologies. IEEE Transactions on Electron Devices, 2012, 59, 2057-2063.	1.6	44
10	Optimizing Multi-GPU Parallelization Strategies for Deep Learning Training. IEEE Micro, 2019, 39, 91-101.	1.8	43
11	Toward a systematic-variation aware timing methodology. , 2004, , .		42
12	Mask assignment and synthesis of DSA-MP hybrid lithography for sub-7nm contacts/vias. , 2015, , .		40
13	Write Error Rate and Read Disturbance in Electric-Field-Controlled Magnetic Random-Access Memory. IEEE Magnetics Letters, 2017, 8, 1-5.	0.6	37
14	DDRO: A novel performance monitoring methodology based on design-dependent ring oscillators. , 2012, , .		36
15	Performance-impact limited area fill synthesis. , 2003, , .		33
16	Latency, Bandwidth and Power Benefits of the SuperCHIPS Integration Scheme. , 2017, , .		33
17	SlackProbe: A Low Overhead In Situ On-line Timing Slack Monitoring Methodology. , 2013, , .		30
18	Physically Justifiable Die-Level Modeling of Spatial Variation in View of Systematic Across Wafer Variability. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2011, 30, 388-401.	1.9	29

#	Article	IF	Citations
19	Design and Analysis of Stability-Guaranteed PUFs. IEEE Transactions on Information Forensics and Security, 2018, 13, 978-992.	4.5	29
20	Modeling of non-uniform device geometries for post-lithography circuit analysis. , 2006, , .		27
21	Evaluation of Digital Circuit-Level Variability in Inversion-Mode and Junctionless FinFET Technologies. IEEE Transactions on Electron Devices, 2013, 60, 2186-2193.	1.6	27
22	Analysis and Compact Modeling of Magnetic Tunnel Junctions Utilizing Voltage-Controlled Magnetic Anisotropy. IEEE Transactions on Magnetics, 2018, 54, 1-9.	1.2	27
23	Layout Decomposition and Legalization for Double-Patterning Technology. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2013, 32, 202-215.	1.9	26
24	SlackProbe: A Flexible and Efficient In Situ Timing Slack Monitoring Methodology. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2014, 33, 1168-1179.	1.9	25
25	Power / Capacity Scaling. , 2014, , .		25
26	Architecting Waferscale Processors - A GPU Case Study. , 2019, , .		25
27	Wafer Topography-Aware Optical Proximity Correction. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2006, 25, 2747-2756.	1.9	23
28	Detailed placement for improved depth of focus and CD control. , 2005, , .		22
29	Variation-aware speed binning of multi-core processors. , 2010, , .		22
30	Synthesis and Analysis of Design-Dependent Ring Oscillator (DDRO) Performance Monitors. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 2117-2130.	2.1	22
31	Merits of cellwise model-based OPC. , 2004, , .		20
32	VarEMU: An emulation testbed for variability-aware software. , 2013, , .		20
33	Hardware Variability-Aware Duty Cycling for Embedded Sensors. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 1000-1012.	2.1	19
34	ARGO: Aging-aware GPGPU register file allocation. , 2013, , .		19
35	Toward through-process layout quality metrics. , 2005, , .		18
36	ViPZonE. , 2012, , .		18

#	Article	IF	Citations
37	DRE: A Framework for Early Co-Evaluation of Design Rules, Technology Choices, and Layout Methodologies. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2012, 31, 1379-1392.	1.9	18
38	Routing-aware scan chain ordering. ACM Transactions on Design Automation of Electronic Systems, 2005, 10, 546-560.	1.9	17
39	Physically justifiable die-level modeling of spatial variation in view of systematic across wafer variability. , 2009, , .		16
40	Eyecharts. , 2010, , .		15
41	Single-Mask Double-Patterning Lithography for Reduced Cost and Improved Overlay Control. IEEE Transactions on Semiconductor Manufacturing, 2011, 24, 93-103.	1.4	15
42	Power Variability in Contemporary DRAMs. IEEE Embedded Systems Letters, 2012, 4, 37-40.	1.3	15
43	A Word Line Pulse Circuit Technique for Reliable Magnetoelectric Random Access Memory. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 2027-2034.	2.1	15
44	Tunneling Negative Differential Resistance-Assisted STT-RAM for Efficient Read and Write Operations. IEEE Transactions on Electron Devices, 2017, 64, 121-129.	1.6	15
45	A Case for Packageless Processors. , 2018, , .		15
46	Measuring the Impact of Memory Errors on ApplicationÂ Performance. IEEE Computer Architecture Letters, 2017, 16, 51-55.	1.0	14
47	ACOUSTIC: Accelerating Convolutional Neural Networks through Or-Unipolar Skipped Stochastic Computing. , 2020, , .		14
48	Design Space Exploration for Chiplet-Assembly-Based Processors. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 1062-1073.	2.1	14
49	Lithography simulation-based full-chip design analyses. , 2006, , .		13
50	Design-overlay interactions in metal double patterning. , 2009, , .		13
51	Electrical Modeling of Lithographic Imperfections. , 2010, , .		13
52	<title>A novel methodology for triple/multiple-patterning layout decomposition</title>. Proceedings of SPIE, 2012, , .	0.8	13
53	AppAdapt: Opportunistic Application Adaptation in Presence of Hardware Variation. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2012, 20, 1986-1996.	2.1	13
54	Multi-Layer Memory Resiliency. , 2014, , .		13

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55	Incorporating DSA in multipatterning semiconductor manufacturing technologies. Proceedings of SPIE, 2015, , .	0.8	13
56	MTJ variation monitor-assisted adaptive MRAM write. , 2016, , .		13
57	A framework for early and systematic evaluation of design rules. , 2009, , .		13
58	Efficient Additive Statistical Leakage Estimation. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2009, 28, 1777-1781.	1.9	12
59	VaMV: Variability-aware Memory Virtualization. , 2012, , .		12
60	Software-Defined Error-Correcting Codes. , 2016, , .		12
61	Low-Cost Memory Fault Tolerance for IoT Devices. Transactions on Embedded Computing Systems, 2017, 16, 1-25.	2.1	12
62	Software adaptation in quality sensitive applications to deal with hardware variability. , 2010, , .		12
63	DPCS. Transactions on Architecture and Code Optimization, 2015, 12, 1-26.	1.6	12
64	Variability-aware duty cycle scheduling in long running embedded sensing systems. , 2011, , .		11
65	LEDPUF: Stability-guaranteed physical unclonable functions through locally enhanced defectivity. , 2016, , .		11
66	Source Line Sensing in Magneto-Electric Random-Access Memory to Reduce Read Disturbance and Improve Sensing Margin. IEEE Magnetics Letters, 2016, 7, 1-5.	0.6	11
67	Quantifying Error in Dynamic Power Estimation of CMOS Circuits. Analog Integrated Circuits and Signal Processing, 2005, 42, 253-264.	0.9	10
68	Design dependent process monitoring for back-end manufacturing cost reduction. , 2010, , .		10
69	A methodology for the early exploration of design rules for multiple-patterning technologies. , 2012, , .		10
70	Design-Aware Defect-Avoidance Floorplanning of EUV Masks. IEEE Transactions on Semiconductor Manufacturing, 2013, 26, 111-124.	1.4	10
71	NSF expedition on variability-aware software: Recent results and contributions. IT - Information Technology, 2015, 57, 181-198.	0.6	10
72	X-Mem: A cross-platform and extensible memory characterization tool for the cloud. , 2016, , .		10

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73	Hybrid VC-MTJ/CMOS non-volatile stochastic logic for efficient computing. , 2017, , .		10
74	Designing a 2048-Chiplet, 14336-Core Waferscale Processor. , 2021, , .		10
75	4F optical neural network acceleration: an architecture perspective. , 2022, , .		10
76	Investigation of diffusion rounding for post-lithography analysis. , 2008, , .		8
77	Electrical metrics for lithographic line-end tapering. Proceedings of SPIE, 2008, , .	0.8	8
78	Incremental gate sizing for late process changes. , 2010, , .		8
79	Layout pattern-driven design rule evaluation. Journal of Micro/ Nanolithography, MEMS, and MOEMS, 2014, 13, 043018.	1.0	8
80	BTI-Gater: An Aging-Resilient Clock Gating Methodology. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2014, 4, 180-189.	2.7	8
81	MEMRES: A Fast Memory System Reliability Simulator. IEEE Transactions on Reliability, 2016, 65, 1783-1797.	3.5	8
82	Parity++: Lightweight Error Correction for Last Level Caches. , 2018, , .		8
83	Adaptive MRAM Write and Read with MTJ Variation Monitor. IEEE Transactions on Emerging Topics in Computing, 2021, 9, 402-413.	3.2	8
84	Electro-Optical Hybrid Fourier Neural Network with Amplitude-Only Modulation. , 2020, , .		8
85	Shaping gate channels for improved devices. , 2008, , .		7
86	A framework for double patterning-enabled design. , 2011, , .		7
87	Defect-aware reticle floorplanning for EUV masks. , 2011, , .		7
88	Comprehensive defect avoidance framework for mitigating EUV mask defects. Proceedings of SPIE, 2014, , .	0.8	7
89	Comprehensive die-level assessment of design rules and layouts. , 2014, , .		7
90	ViPZonE: Hardware Power Variability-Aware Virtual Memory Management for Energy Savings. IEEE Transactions on Computers, 2015, 64, 1483-1496.	2.4	7

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91	PROCEED: A Pareto Optimization-Based Circuit-Level Evaluator for Emerging Devices. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 192-205.	2.1	7
92	Wafer topography-aware optical proximity correction for better DOF margin and CD control. , 2005, , .		6
93	Modeling OPC complexity for design for manufacturability. , 2005, 5992, 612.		6
94	Modeling edge placement error distribution in standard cell library. , 2006, 6156, 265.		6
95	What is process window?. ACM SIGDA Newsletter, 2010, 40, 1-1.	0.0	6
96	Evaluating Statistical Power Optimization. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2010, 29, 1750-1762.	1.9	6
97	Variability-aware memory management for nanoscale computing. , 2013, , .		6
98	Discrete sizing for leakage power optimization in physical design. ACM Transactions on Design Automation of Electronic Systems, 2013, 18, 1-11.	1.9	6
99	Role of Design in Multiple Patterning: Technology Development, Design Enablement and Process Control. , 2013, , .		6
100	PROCEED: A pareto optimization-based circuit-level evaluator for emerging devices. , 2014, , .		6
101	Efficient Layout Generation and Design Evaluation of Vertical Channel Devices. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, 35, 1449-1460.	1.9	6
102	Assessing Benefits of a Buried Interconnect Layer in Digital Designs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 346-350.	1.9	6
103	Leveraging nMOS Negative Differential Resistance for Low Power, High Reliability Magnetic Memory. IEEE Transactions on Electron Devices, 2017, 64, 4084-4090.	1.6	6
104	Context-Aware Resiliency: Unequal Message Protection for Random-Access Memories. IEEE Transactions on Information Theory, 2019, 65, 6146-6159.	1.5	6
105	SLATE: A Secure Lightweight Entity Authentication Hardware Primitive. IEEE Transactions on Information Forensics and Security, 2020, 15, 276-285.	4.5	6
106	Multi-Story Power Distribution Networks for GPUs. , 2016, , .		6
107	Million-channel parallelism Fourier-optic convolutional filter and neural network processor. , 2020, , .		6
108	3PXNet. Transactions on Embedded Computing Systems, 2020, 19, 1-23.	2.1	6

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109	Investigation of performance metrics for interconnect stack architectures. , 2004, , .		5
110	On Electrical Modeling of Imperfect Diffusion Patterning. , 2010, , .		5
111	Accurate and inexpensive performance monitoring for variability-aware systems. , 2014, , .		5
112	Efficient layout generation and evaluation of vertical channel devices. , 2014, , .		5
113	Mask Assignment and DSA Grouping for DSA-MP Hybrid Lithography for Sub-7 nm Contact/Via Holes. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 913-926.	1.9	5
114	Context-aware resiliency: Unequal message protection for random-access memories. , 2017, , .		5
115	GEO: Generation and Execution Optimized Stochastic Computing Accelerator for Neural Networks. , 2021, , .		5
116	Interaction and balance of mask write time and design RET strategies. , 2005, , .		4
117	Manufacturing-aware design methodology for assist feature correctness. , 2005, , .		4
118	Accounting for non-linear dependence using function driven component analysis. , 2009, , .		4
119	Design-Aware Mask Inspection. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2012, 31, 690-702.	1.9	4
120	Towards analyzing and improving robustness of software applications to intermittent and permanent faults in hardware. , 2013, , .		4
121	A framework for exploring the interaction between design rules and overlay control. Proceedings of SPIE, 2013, , .	0.8	4
122	ECO cost measurement and incremental gate sizing for late process changes. ACM Transactions on Design Automation of Electronic Systems, 2013, 18, 1-11.	1.9	4
123	Comprehensive defect avoidance framework for mitigating extreme ultraviolet mask defects. Journal of Micro/ Nanolithography, MEMS, and MOEMS, 2014, 13, 043005.	1.0	4
124	Variability Expeditions: A Retrospective. IEEE Design and Test, 2019, 36, 65-67.	1.1	4
125	Reverse Engineering for 2.5-D Split Manufactured ICs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 3128-3133.	1.9	4
126	Taming pattern and focus variation in VLSI design. , 2004, , .		3

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127	Standard cell library optimization for leakage reduction. , 2006, , .		3
128	Self-Compensating Design for Reduction of Timing and Leakage Sensitivity to Systematic Pattern-Dependent Variation. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2007, 26, 1614-1624.	1.9	3
129	<title>Design-of-experiments based design rule optimization</title>. Proceedings of SPIE, 2012, , .	0.8	3
130	Discrete Circuit Optimization. Foundations and Trends in Electronic Design Automation, 2012, 6, 1-120.	1.0	3
131	Framework for exploring the interaction between design rules and overlay control. Journal of Micro/ Nanolithography, MEMS, and MOEMS, 2013, 12, 033014.	1.0	3
132	Statistical timing and power analysis of VLSI considering non-linear dependence. The Integration VLSI Journal, 2014, 47, 487-498.	1.3	3
133	Benchmarking of Mask Fracturing Heuristics. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 170-183.	1.9	3
134	Implementation of stable PUFs using gate oxide breakdown. , 2017, , .		3
135	Performance-impact limited-area fill synthesis. , 2003, , .		3
136	Compression with multi-ECC. , 2019, , .		3
137	Pathfinding for 2.5D interconnect technologies. , 2020, , .		3
138	Toward performance-driven reduction of the cost of RET-based lithography control. , 2003, , .		2
139	Enhanced resist and etch CD control by design perturbation. , 2005, , .		2
140	Single-mask double-patterning lithography. , 2009, , .		2
141	Design-aware mask inspection. , 2010, , .		2
142	Underdesigned and Opportunistic Computing. , 2011, , .		2
143	Benchmarking of mask fracturing heuristics. , 2014, , .		2
144	EUV-CDA: Pattern shift aware critical density analysis for EUV mask layouts. , 2014, , .		2

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145	Effective model-based mask fracturing for mask cost reduction. , 2015, , .		2
146	An Evaluation Framework for Nanotransfer Printing-Based Feature-Level Heterogeneous Integration in VLSI Circuits. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 1858-1870.	2.1	2
147	Assessing Layout Density Benefits of Vertical Channel Devices. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 3211-3215.	1.9	2
148	I/O Architecture, Substrate Design, and Bonding Process for a Heterogeneous Dielet-Assembly based Waferscale Processor. , 2021, , .		2
149	Dynamic programming approach to adaptive slicing for optimization under a global volumetric error constraint. , 2018, , .		2
150	Relaxing LER requirement in EUV lithography. , 2018, , .		2
151	On the futility of statistical power optimization. , 2009, , .		1
152	On comparing conventional and electrically driven OPC techniques. , 2009, , .		1
153	Measurement and optimization of electrical process window. Proceedings of SPIE, 2010, , .	0.8	1
154	Design-Dependent Process Monitoring for Wafer Manufacturing and Test Cost Reduction. IEEE Transactions on Semiconductor Manufacturing, 2012, 25, 447-459.	1.4	1
155	Pattern-restricted design at 10nm and beyond. , 2014, , .		1
156	Layout pattern-driven design rule evaluation. Proceedings of SPIE, 2014, , .	0.8	1
157	Evaluating and exploiting impacts of dynamic power management schemes on system reliability. , 2015, , .		1
158	Hardware Reliability margining for the dark silicon era. , 2016, , .		1
159	Technology path-finding framework for directed-self assembly for via layers. Journal of Micro/Nanolithography, MEMS, and MOEMS, 2017, 16, 013505.	1.0	1
160	Advanced Packaging and Heterogeneous Integration to Reboot Computing. , 2017, , .		1
161	Error Correction and Detection for Computing Memories Using System Side Information. , 2018, , .		1
162	Defect avoidance for extreme ultraviolet mask defects using intentional pattern deformation. , 2018, , .		1

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163	Lightweight Software-Defined Error Correction for Memories. Embedded Systems, 2021, , 207-232.	0.6	1
164	SAME-Infer: Software Assisted Memory Resilience for Efficient Inference at the Edge. , 2020, , .		1
165	A Calibration-Free In-Memory True Random Number Generator Using Voltage-Controlled MRAM. , 2021, , .		1
166	LAC: Learned Approximate Computing. , 2022, , .		1
167	Joining the design and mask flows for better and cheaper masks. , 2004, , .		0
168	Improving OPC quality via interactions within the design-to-manufacturing flow (Invited Paper). , 2005, 5853, 131.		0
169	Self-compensating design for reduction of timing and leakage sensitivity to systematic pattern dependent variation. , 2006, , .		0
170	Design and use of tweakable devices for future logic implementation. , 2008, , .		0
171	On confidence in characterization and application of variation models. , 2010, , .		0
172	Collaborative research on emerging technologies and design. Proceedings of SPIE, 2011, , .	0.8	0
173	Impact of range and precision in technology on cell-based design. , 2012, , .		0
174	Parametric Hierarchy Recovery in Layout Extracted Netlists. , 2012, , .		0
175	O(n) layout-coloring for multiple-patterning lithography and conflict-removal using compaction. , 2012, , .		0
176	Design for nanoscale patterning. , 2013, , .		0
177	Minimizing clock domain crossing in Network on Chip interconnect. , 2014, , .		0
178	Technology path-finding for directed self-assembly for via layers. , 2017, , .		0
179	System-Level Dynamic Variation Margining in Presence of Monitoring and Actuation. IEEE Embedded Systems Letters, 2017, 9, 85-88.	1.3	0
180	Design Impacts of Back-End-of-Line Line Edge Roughness. IEEE Transactions on Semiconductor Manufacturing, 2020, 33, 32-41.	1.4	0

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181	A Calibration-Free In-Memory True Random Number Generator Using Voltage-Controlled MRAM. , 2021, , .		0
182	Fourier Optic Convolutional Neural Network. , 2021, , .		0
183	Fourier Optical Convolutional Neural Network Accelerator. , 2021, , .		0
184	High Throughput Multi-kernel Fourier Optic Classifier. , 2021, , .		0
185	DRDebug: Automated Design Rule Debugging. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2023, 42, 606-615.	1.9	0