Eunah Ko

List of Publications by Year
in descending order

11 papers	375 citations	1307594 7 h-index	1372567 10 g-index
11 all docs	11 docs citations	11 times ranked	412 citing authors

#	Article	IF	Citations
1	Optimization of double metal-gate InAs/Si heterojunction nanowire TFET. Semiconductor Science and Technology, 2020, 35, 075024.	2.0	8
2	Steep Slope Silicon-on-Insulator Field Effect Transistor with Negative Capacitance: Analysis on Hysteresis. Journal of Nanoscience and Nanotechnology, 2019, 19, 6128-6130.	0.9	1
3	Steep Slope Silicon-On-Insulator Feedback Field-Effect Transistor: Design and Performance Analysis. IEEE Transactions on Electron Devices, 2019, 66, 286-291.	3.0	33
4	Analysis on the Operation of Negative Differential Resistance FinFET With Pb(Zr_{0.52}Ti_{0.48})O₃ Threshold Selector. IEEE Transactions on Electron Devices, 2018, 65, 19-22.	3.0	13
5	Super steep-switching (SS â‰ˆ 2 mV/decade) phase-FinFET with Pb(Zr0.52Ti0.48)O3 threshold switching device. Applied Physics Letters, 2018, 113, .	3.3	8
6	Steep switching devices for low power applications: negative differential capacitance/resistance field effect transistors. Nano Convergence, 2018, 5, 2.	12.1	60
7	Negative Capacitance FinFET With Sub-20-mV/decade Subthreshold Slope and Minimal Hysteresis of 0.48 V. IEEE Electron Device Letters, 2017, 38, 418-421.	3.9	100
8	Effective drive current in steep slope FinFET (vs. conventional FinFET). Applied Physics Letters, 2017, 111, .	3.3	5
9	Sub-60-mV/decade Negative Capacitance FinFET With Sub-10-nm Hafnium-Based Ferroelectric Capacitor. IEEE Journal of the Electron Devices Society, 2017, 5, 306-309.	2.1	57
10	Layout engineering to suppress hysteresis of negative capacitance FinFET. , 2017, , .		0
11	Vertical Tunnel FET: Design Optimization With Triple Metal-Gate Layers. IEEE Transactions on Electron Devices, 2016, 63, 5030-5035.	3.0	90