

Adib Abrishamifar

List of Publications by Year in descending order

Source: <https://exaly.com/author-pdf/534928/publications.pdf>

Version: 2024-02-01

74
papers

639
citations

840776

11
h-index

677142

22
g-index

74
all docs

74
docs citations

74
times ranked

707
citing authors

#	ARTICLE	IF	CITATIONS
1	A modified SOGI-FLL algorithm with DC-offset rejection improvement for single-phase inverter applications. International Journal of Dynamics and Control, 2022, 10, 2020-2033.	2.5	1
2	An Improved Threefold Interleaved PFC Circuit With Better Voltage Profile and Optimizing Current-Sharing Method. Canadian Journal of Electrical and Computer Engineering, 2021, 44, 253-260.	2.0	1
3	A Simple and Adjustable Technique for Effective Linearization of Power Amplifiers Using Harmonic Injection. IEEE Access, 2021, 9, 37287-37296.	4.2	4
4	A Hybrid SMC Strategy for Sequential Switching Shunt Regulator. , 2021, , .		0
5	An Optimized Zero-Current, Zero-Voltage, and Three-Level DC-DC Converter. Canadian Journal of Electrical and Computer Engineering, 2021, 44, 216-222.	2.0	2
6	A wideband quasi-asymmetric Doherty power amplifier with a two-section matching-phase difference compensator network design using GaAs technology. Analog Integrated Circuits and Signal Processing, 2020, 105, 359-370.	1.4	0
7	Automatic tuning of the Class E power amplifier applied in inductive links during coil separation variations. AEU - International Journal of Electronics and Communications, 2020, 124, 153337.	2.9	2
8	A New Carrier-Based Pulse Width Modulation Scheme with Reduced Output Voltage Total Harmonic Distortion for Multi-Level Inverters. IETE Journal of Research, 2020, , 1-12.	2.6	4
9	Evaluating a Methodology for Designing CNFET-Based Ternary Circuits. Circuits, Systems, and Signal Processing, 2020, 39, 5039-5058.	2.0	9
10	On the design of robust, low power with high noise immunity quaternary circuits. Microelectronics Journal, 2020, 102, 104774.	2.0	11
11	A Systematic Methodology for Optimal Design of Wireless Power Transfer System Using Genetic Algorithm. Energies, 2020, 13, 383.	3.1	8
12	A Five-Switch Active NPC With Low Output Voltage THD For Photovoltaic Applications. , 2019, , .		0
13	A New Method for Design of CNFET-Based Quaternary Circuits. Circuits, Systems, and Signal Processing, 2019, 38, 2588-2606.	2.0	20
14	A high precision analog multiplexer for multi-channel neural recording micro-systems. Microelectronics Journal, 2018, 71, 8-18.	2.0	0
15	Low-Power High-Speed Analog Multiplier/Divider Based on a New Current Squarer Circuit. Arabian Journal for Science and Engineering, 2018, 43, 2909-2918.	3.0	20
16	A novel analog switch for high-precision switched-capacitor applications. International Journal of Circuit Theory and Applications, 2018, 46, 764-778.	2.0	6
17	A New Topology of Switched-Capacitor Multilevel Inverter for Single-Phase Grid-Connected with Eliminating Leakage Current. , 2018, , .		9
18	An improved integrated control modeling of a high-power density interleaved non-inverting buck-boost DC-DC converter. World Journal of Engineering, 2018, 15, 688-699.	1.6	5

#	ARTICLE	IF	CITATIONS
19	Experimentally evaluation and comparison of control methods applied to three phase four-leg inverter for stand-alone applications. , 2018, , .		2
20	A 5-level modified full-bridge stand-alone inverter with reduced number of switches. International Transactions on Electrical Energy Systems, 2018, 28, e2638.	1.9	21
21	A novel OTA compensation approach suitable for CT $\hat{\imath}$ modulators. International Journal of Circuit Theory and Applications, 2018, 46, 2248-2265.	2.0	1
22	A Simple and Efficient Charge Injection Error Compensation Structure for MOS Sampling Switches. Journal of Circuits, Systems and Computers, 2018, 27, 1850130.	1.5	5
23	Extrinsic Rashba spin $\hat{\imath}$ orbit coupling effect on silicene spin polarized field effect transistors. Journal of Physics Condensed Matter, 2017, 29, 145501.	1.8	26
24	System level design and analysis of a fourth $\hat{\imath}$ order continuous $\hat{\imath}$ time delta $\hat{\imath}$ sigma modulator using relaxed gain $\hat{\imath}$ bandwidth amplifiers. International Journal of Circuit Theory and Applications, 2017, 45, 1576-1599.	2.0	3
25	Simple and efficient design and control of the single phase PWM rectifier for UPS applications. , 2017, , .		4
26	A 500 $\hat{\imath}$ MHz low offset fully differential latched comparator. Analog Integrated Circuits and Signal Processing, 2017, 92, 233-245.	1.4	2
27	An efficient interleaved high step-up converter with winding-cross-coupled inductor and common active clamp for photovoltaic applications. , 2017, , .		1
28	An inductorless wideband LNA with a new noise canceling technique. Turkish Journal of Electrical Engineering and Computer Sciences, 2017, 25, 1147-1153.	1.4	3
29	Improved equations of switching loss and conduction loss in SPWM multilevel inverters. , 2016, , .		23
30	Design procedure and experimental validation of a 30kVA DSP-based PWM rectifier. , 2016, , .		1
31	A search algorithm to design optimum CT $\hat{\imath}$ modulator with finite GBW amplifiers. , 2016, , .		0
32	A novel method for real-time selective harmonic elimination in five-level converters. , 2016, , .		4
33	Implementation of the first commercial medium power active front end transformerless uninterruptible power supply made in Iran. , 2016, , .		2
34	Elimination of low order harmonics in nine-level cascaded H-bridge converter. , 2016, , .		0
35	A new simple structure PLL for both single and three phase applications. International Journal of Electrical Power and Energy Systems, 2016, 74, 118-125.	5.5	14
36	A High-Linear CMOS Down Conversion Mixer Using Adjusting the Second and Third-Order Harmonic in Transconductance Stage. Journal of Circuits, Systems and Computers, 2015, 24, 1550002.	1.5	2

#	ARTICLE	IF	CITATIONS
37	A switched-capacitor multilevel inverter for high AC power systems with reduced ripple loss using SPWM technique. , 2015, , .		21
38	A FAST AND LOW SETTling ERROR CONTINUOUS-TIME COMMON-MODE FEEDBACK CIRCUIT BASED ON DIFFERENTIAL DIFFERENCE AMPLIFIER. Journal of Circuits, Systems and Computers, 2014, 23, 1450065.	1.5	5
39	A new scheme of multilevel inverter with charge balancing control and minimum number of switches. , 2014, , .		0
40	A modified synchronous detection method with power factor control and suitable performance under non-ideal grid voltage applicable for three phase active power filters. , 2014, , .		0
41	A 200 MHz-to-1.4 GHz fast-locking pulse width control loop. International Journal of Electronics, 2014, 101, 341-353.	1.4	0
42	Evaluation of different positive sequence detection structures applied to grid-connected systems. , 2014, , .		1
43	Designing 3-phase inverters with Δ/Y output isolation transformer. , 2014, , .		0
44	A cross coupled low phase noise oscillator using an output swing enhancement technique. Microelectronics Journal, 2014, 45, 1008-1013.	2.0	11
45	Fast SVM for a five level flying capacitor drive with overvoltage reduction. , 2013, , .		1
46	NONLINEAR OBSERVER FOR INDUCTION MOTOR TO IMPROVE EFFICIENCY AND DYNAMIC STABILITY ANALYSIS IN FOC METHOD. Journal of Circuits, Systems and Computers, 2012, 21, 1250011.	1.5	2
47	Current controlled current differential current conveyor: a novel building block for analog signal processing. IEICE Electronics Express, 2012, 9, 104-110.	0.8	4
48	Fixed Switching Frequency Sliding Mode Control for Single-Phase Unipolar Inverters. IEEE Transactions on Power Electronics, 2012, 27, 2507-2514.	7.9	189
49	Low-frequency current ripple reduction in front-end boost converter with single-phase inverter load. IET Power Electronics, 2012, 5, 1676-1683.	2.1	36
50	Analysis and design of the true piecewise approximation logarithmic amplifiers. Analog Integrated Circuits and Signal Processing, 2012, 72, 193-203.	1.4	13
51	A low voltage low power CMOS analog multiplier. , 2011, , .		2
52	Fixed frequency sliding mode controller for the buck converter. , 2011, , .		2
53	Flying Capacitor DTC Drive with Reductions in Common Mode Voltage and Stator Overvoltage. Journal of Power Electronics, 2011, 11, 512-519.	1.5	4
54	A novel current conveyor with high functionality and optimized ports. IEICE Electronics Express, 2010, 7, 1480-1485.	0.8	5

#	ARTICLE	IF	CITATIONS
55	A novel CMOS all-pass tunable phase shifter for phased array systems. , 2009, , .		0
56	A new high speed, low power adder; using hybrid analog-digital circuits. , 2009, , .		2
57	A low voltage CMOS analog multiplier with high linearity. , 2009, , .		2
58	A novel ultra low-leakage switch for switched capacitor circuits. , 2009, , .		3
59	Investigating the linearity of MOSFET-only switched-capacitor ΔΣ modulators under low-voltage condition. , 2009, , .		1
60	A programmable true piecewise approximation logarithmic amplifier. , 2009, , .		5
61	A novel CMOS all-pass tunable phase shifter. , 2009, , .		0
62	A new CMOS all-pass phase shifter for phased array systems. IEICE Electronics Express, 2009, 6, 504-510.	0.8	6
63	A low voltage highly linear CMOS up conversion mixer based on current conveyor. IEICE Electronics Express, 2009, 6, 930-935.	0.8	10
64	Comparison of Electroanesthesia with Chemical Anesthesia (MS222 and Clove Oil) in Rainbow Trout (Oncorhynchus mykiss) using Plasma Cortisol and Glucose Responses as Physiological Stress Indicators. Asian Journal of Animal and Veterinary Advances, 2009, 4, 306-313.	0.0	28
65	Generation and detection of nano ultrasound waves with a multiple strained layer structure. Optical and Quantum Electronics, 2008, 40, 577-586.	3.3	2
66	Low power and high gain current reuse LNA with modified input matching and inter-stage inductors. Microelectronics Journal, 2008, 39, 1534-1537.	2.0	20
67	A novel peak and deep current mode control for two switches buck-boost converter. IEEE Applied Power Electronics Conference and Exposition, 2008, , .	0.0	3
68	A 5.5-GHz 3mW LNA and inductive degenerative CMOS LNA noise figure calculation. , 2008, , .		9
69	A current source power supply for driving of series connected power switch. , 2008, , .		1
70	Jitter peaking investigation in charge pump based clock and data recovery circuits. , 2007, , .		3
71	An FPGA-based irrational decimator for digital receivers. , 2007, , .		3
72	A low-power and high-gain fully integrated CMOS LNA. Microelectronics Journal, 2007, 38, 1150-1155.	2.0	23

#	ARTICLE	IF	CITATIONS
73	An DSTATCOM for Compensating Different Abnormal Line Voltage and Nonlinear Load. , 2006, , .		4
74	A Novel Wide-Range Delay Cell for DLLs. , 2006, , .		2