

Francesca Palumbo

List of Publications by Year in descending order

Source: <https://exaly.com/author-pdf/5341510/publications.pdf>

Version: 2024-02-01

55
papers

474
citations

1040056

9
h-index

839539

18
g-index

55
all docs

55
docs citations

55
times ranked

387
citing authors

#	ARTICLE	IF	CITATIONS
1	The Multi-Dataflow Composer tool: An open-source tool suite for optimized coarse-grain reconfigurable hardware accelerators and platform design. <i>Microprocessors and Microsystems</i> , 2021, 80, 103326.	2.8	6
2	Unmanned Vehicles in Smart Farming: a Survey and a Glance at Future Horizons. , 2021, , .		4
3	Design and management of image processing pipelines within CPS: Acquired experience towards the end of the FitOptiVis ECSEL Project. <i>Microprocessors and Microsystems</i> , 2021, 87, 104350.	2.8	3
4	Design and management of image processing pipelines within CPS: 2 years of experience from the FitOptiVis ECSEL Project. , 2020, , .		5
5	Feasibility Study and Porting of the Damped Least Square Algorithm on FPGA. <i>IEEE Access</i> , 2020, 8, 175483-175500.	4.2	1
6	Hardware/Software Self-adaptation in CPS: The CERBERO Project Approach. <i>Lecture Notes in Computer Science</i> , 2019, , 416-428.	1.3	4
7	CERBERO: Cross-layer modEl-based fRamework for multi-oBjective dEsign of reconfigurable systems in unceRtain hybRid enviroNments. , 2019, , .		4
8	NeuPow. , 2019, , .		4
9	Preface to the Special Issue on Methods, Tools, and Architectures for Signal and Image Processing. <i>Journal of Signal Processing Systems</i> , 2019, 91, 701-702.	2.1	0
10	Optimization and deployment of CNNs at the edge. , 2019, , .		10
11	The FitOptiVis ECSEL project. , 2019, , .		28
12	Editorial: Special Issue on Computing Frontiers. <i>Journal of Signal Processing Systems</i> , 2019, 91, 273-273.	2.1	0
13	An integrated hardware/software design methodology for signal processing systems. <i>Journal of Systems Architecture</i> , 2019, 93, 1-19.	4.3	18
14	Dataflow-Functional High-Level Synthesis for Coarse-Grained Reconfigurable Accelerators. <i>IEEE Embedded Systems Letters</i> , 2019, 11, 69-72.	1.9	6
15	Dataflow Modeling for Reconfigurable Signal Processing Systems. , 2019, , 787-824.		2
16	Challenging CPS Trade-off Adaptivity with Coarse-Grained Reconfiguration. <i>Lecture Notes in Electrical Engineering</i> , 2019, , 57-63.	0.4	2
17	Architecture-aware design and implementation of CNN algorithms for embedded inference: the ALOHA project. , 2018, , .		1
18	Multi-Grain Reconfiguration for Advanced Adaptivity in Cyber-Physical Systems. , 2018, , .		3

#	ARTICLE	IF	CITATIONS
19	Power-Awareness in Coarse-Grained Reconfigurable Multi-Functional Architectures: a Dataflow Based Strategy. Journal of Signal Processing Systems, 2017, 87, 81-106.	2.1	14
20	Challenging the Best HEVC Fractional Pixel FPGA Interpolators With Reconfigurable and Multifrequency Approximate Computing. IEEE Embedded Systems Letters, 2017, 9, 65-68.	1.9	15
21	Feasibility study of real-time spiking neural network simulations on a swarm intelligence based digital architecture. , 2017, , .		1
22	Hardware design methodology using lightweight dataflow and its integration with low power techniques. Journal of Systems Architecture, 2017, 78, 15-29.	4.3	5
23	Real-Time neural signal decoding on heterogeneous MPSocs based on VLIW ASIPs. Journal of Systems Architecture, 2017, 76, 89-101.	4.3	2
24	Adaptive software-augmented hardware reconfiguration with dataflow design automation. , 2017, , .		0
25	An FPGA Platform for Real-Time Simulation of Spiking Neuronal Networks. Frontiers in Neuroscience, 2017, 11, 90.	2.8	69
26	Modelling and Automated Implementation of Optimal Power Saving Strategies in Coarse-Grained Reconfigurable Architectures. Journal of Electrical and Computer Engineering, 2016, 2016, 1-27.	0.9	3
27	Demo: Reconfigurable Platform Composer Tool. , 2016, , .		0
28	Low power design methodology for signal processing systems using lightweight dataflow techniques. , 2016, , .		1
29	Dataflow-Based Design of Coarse-Grained Reconfigurable Platforms. , 2016, , .		2
30	Runtime Energy versus Quality Tuning in Motion Compensation Filters for HEVC. IFAC-PapersOnLine, 2016, 49, 145-152.	0.9	5
31	On-the-fly adaptivity for process networks over shared-memory platforms. Microprocessors and Microsystems, 2016, 46, 240-254.	2.8	3
32	Adaptable AES implementation with power-gating support. , 2016, , .		3
33	Automated Design Flow for Multi-Functional Dataflow-Based Platforms. Journal of Signal Processing Systems, 2016, 85, 143-165.	2.1	14
34	Power and clock gating modelling in coarse grained reconfigurable systems. , 2016, , .		8
35	MPSocs for real-time neural signal decoding: A low-power ASIP-based implementation. Microprocessors and Microsystems, 2016, 43, 67-80.	2.8	4
36	Early Stage Automatic Strategy for Power-Aware Signal Processing Systems Design. Journal of Signal Processing Systems, 2016, 82, 311-329.	2.1	0

#	ARTICLE	IF	CITATIONS
37	Power modelling for saving strategies in coarse grained reconfigurable systems. , 2015, , .		1
38	Exploring custom heterogeneous MPSoCs for real-time neural signal decoding. , 2015, , .		2
39	Coarse-grained reconfiguration: dataflow-based power management. IET Computers and Digital Techniques, 2015, 9, 36-48.	1.2	12
40	Reconfigurable coprocessors synthesis in the MPEG-RVC domain. , 2015, , .		8
41	Computing Swarms for Self-Adaptiveness and Self-Organization in Floating-Point Array Processing. ACM Transactions on Autonomous and Adaptive Systems, 2015, 10, 1-34.	0.8	1
42	Automated power gating methodology for dataflow-based reconfigurable systems. , 2015, , .		6
43	Automatic generation of dataflow-based reconfigurable co-processing units. , 2014, , .		2
44	Power-awareness in coarse-grained reconfigurable designs: A dataflow based strategy. , 2014, , .		3
45	The multi-dataflow composer tool: generation of on-the-fly reconfigurable platforms. Journal of Real-Time Image Processing, 2014, 9, 233-249.	3.5	21
46	DSE and profiling of multi-context coarse-grained reconfigurable systems. , 2013, , .		13
47	A coarse-grained reconfigurable approach for low-power spike sorting architectures. , 2013, , .		13
48	The Multi-Dataflow Composer tool: A runtime reconfigurable HDL platform composer. , 2011, , .		13
49	Towards self-adaptive networks on chip for massively parallel processors. , 2011, , .		0
50	Impact of Half-Duplex and Full-Duplex DMA Implementations on NoC Performance. , 2010, , .		1
51	A Network on Chip Architecture for Heterogeneous Traffic Support with Non-Exclusive Dual-Mode Switching. , 2008, , .		1
52	A Novel Non-exclusive Dual-Mode Architecture for MPSoCs-Oriented Network on Chip Designs. Lecture Notes in Computer Science, 2008, , 96-105.	1.3	5
53	A Surface Tension and Coalescence Model for Dynamic Distributed Resources Allocation in Massively Parallel Processors on-Chip. Studies in Computational Intelligence, 2008, , 335-345.	0.9	5
54	An Off-the-Shelf Instant Contact Casting Device for the Management of Diabetic Foot Ulcers: A randomized prospective trial versus traditional fiberglass cast. Diabetes Care, 2007, 30, 586-590.	8.6	108

#	ARTICLE	IF	CITATIONS
55	Quantum Correlations in a Generalized Spin Star System. Open Systems and Information Dynamics, 2006, 13, 309-314.	1.2	9