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List of Publications by Year
in descending order

7 papers	177 citations	1684188 5 h-index	1872680 6 g-index
7 all docs	7 docs citations	7 times ranked	181 citing authors

#	Article	IF	Citations
1	A Charge-Domain Scalable-Weight In-Memory Computing Macro With Dual-SRAM Architecture for Precision-Scalable DNN Accelerators. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 3305-3316.	5.4	30
2	An Ultra-Low-Power Fully-Static Contention-Free Flip-Flop With Complete Redundant Clock Transition and Transistor Elimination. IEEE Journal of Solid-State Circuits, 2021, 56, 3039-3048.	5.4	11
3	A Redundancy Eliminated Flip-Flop in 28 nm for Low-Voltage Low-Power Applications. IEEE Solid-State Circuits Letters, 2020, 3, 446-449.	2.0	3
4	A Static Contention-Free Differential Flip-Flop in 28nm for Low-Voltage, Low-Power Applications. , 2020, , .		7
5	A Fully Static True-Single-Phase-Clocked Dual-Edge-Triggered Flip-Flop for Near-Threshold Voltage Operation in IoT Applications. IEEE Access, 2020, 8, 40232-40245.	4.2	17
6	A multiple negative differential resistance heterojunction device and its circuit application to ternary static random access memory. Nanoscale Horizons, 2020, 5, 654-662.	8.0	70
7	Double Negative Differential Transconductance Characteristic: From Device to Circuit Application toward Quaternary Inverter. Advanced Functional Materials, 2019, 29, 1905540.	14.9	39