Anuj Grover

List of Publications by Year
in descending order

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38 papers	223 citations	1684188 5 h-index	1872680 6 g-index
39 all docs	39 docs citations	39 times ranked	203 citing authors

#	Article	IF	Citations
1	Resistive Random Access Memory: A Review of Device Challenges. IETE Technical Review (Institution of) Tj ETQq1 1 0.784314 rgBT /O	3.2	56
2	A 460 MHz at 397 mV, 2.6 GHz at 1.3 V, 32 bits VLIW DSP Embedding F MAX Tracking. IEEE Journal of Solid-State Circuits, 2015, 50, 125-136.	5.4	42
3	A 460MHz at 397mV, 2.6GHz at 1.3V, 32b VLIW DSP, embedding F_{MAX} tracking. , 2014, , .		29
4	A 32 kb 0.35â€“1.2 V, 50 MHzâ€“2.5 GHz Bit-Interleaved SRAM With 8 T SRAM Cell and Data Dependent Write Assist in 28-nm UTBB-FDSOI CMOS. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 2438-2447.	5.4	12
5	LoCCo-Based Scan Chain Stitching for Low-Power DFT. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 3227-3236.	3.1	8
6	Comparative analysis of SRAM cells in sub-threshold region in 65nm. , 2015, , .		6
7	A 0.9V 64Mb 6T SRAM cell with Read and Write assist schemes in 65nm LSTP technology. , 2020, , .		6
8	Optimization of a voltage sense amplifier operating in ultra wide voltage range with back bias design techniques in 28nm UTBB FD-SOI technology. , 2013, , .		5
9	Low Standby Power Capacitively Coupled Sense Amplifier for wide voltage range operation of dual rail SRAMs. , 2015, , .		5
10	Area compact 5T portless SRAM cell for high density cache in 65nm CMOS. , 2015, , .		5
11	Static Noise Margin based Yield Modelling of 6T SRAM for Area and Minimum Operating Voltage Improvement using Recovery Techniques. , 2016, , .		5
12	Design of Sense Amplifier for Wide Voltage Range Operation of Split Supply Memories in 22nm HKMG CMOS Technology. , 2020, , .		5
13	ChaCha20-in-Memory for Side-Channel Resistance in IoT Edge-Node Devices. IEEE Open Journal of Circuits and Systems, 2021, 2, 833-842.	1.9	5
14	Statistical Analysis of 64Mb SRAM for Optimizing Yield and Write Performance. , 2015, , .		3
15	Comparative analysis of Sense Amplifiers for SRAM in 65nm CMOS technology. , 2015, , .		3
16	Diagnostic Circuit for Latent Fault Detection in SRAM Row Decoder. , 2020, , .		3
17	Design & Benchmark of Single Bit & Multi Bit Sequential Elements in 65nm for Low Standby Power Consumption. , 2020, , .		3
18	Design and Benchmark of Iso-Stable High Density 4T SRAM cells for 64MB arrays in 65nm LSTP. , 2020, , .		3

#	Article	IF	Citations
19	Floorplan and congestion aware framework for optimal SRAM selection for memory subsystems. , 2015, , .		2
20	An effective test methodology enabling detection of weak bits in SRAMs: Case study in 28nm FDSOI. , 2016, , .		2
21	A New Sense Amplifier Topology with Improved Performance for High Speed SRAM Applications. , 2016, , .		2
22	A 0.4ÂµA Offset, 6ns Sensing-time Multi-level Sense Amplifier for Resistive Non-Volatile Memories in 65nm LSTP Technology. , 2021, , .		2
23	Methodology to Estimate Robustness of Layouts of Radiation Hardened Flip-Flops to High Energy Radiations. , 2020, , .		2
24	A method to estimate effectiveness of weak bit test: Comparison of weak pMOS and WL boost based test - 28nm FDSOI implementation. , 2016, , .		1
25	Heterogeneous memory assembly exploration using a floorplan and interconnect aware framework. , 2016, , .		1
26	New stable loadless 6T dual-port SRAM cell design. , 2016, , .		1
27	A 81nW Error Amplifier Design for Ultra Low Leakage Retention Mode Operation of 4Mb SRAM Array in 40nm LSTP Technology. , 2018, , .		1
28	Comparative Analysis and Implementation of Single-ended Sense Amplifier Schemes using 65nm LSTP CMOS Technology. , 2020, , .		1
29	Actively Compensated Read Assist Technique for 0.6 V Operation of 16 Mb High Density SRAM in 65nm LSTP. , 2020, , .		1
30	Charge Scavenging Gate Coupled Hierarchical Bitline Scheme for Ultra-Low Power SRAMs in 65nm LSTP CMOS. , 2021, , .		1
31	Design Of High Density Memory Cell Library For Low Voltage Operation In 65nm LSTP Technology. , 2021, , .		1
32	Scan Chain Adaptation through ECO. , 2016, , .		0
33	A 0.47V-1.17V 32KB Timing Speculative SRAM in 28nm HKMG CMOS. , 2020, , .		0
34	Reduced March iC- Test for Detecting Ageing Induced Faults in Memory Address Decoders. , 2021, , .		0
35	AXI Based Three 8-bit Parallel Input to One Serial Output Converter with Priority Management System and Asynchronous Clocks at Input and Output. , 2020, , .		0
36	300MHz to 500MHz Optimization of ARM Cortex M7 for Sensor Fusion SoCs by using Multi-threshold Libraries and Multi-bit Register cells in 16nm FinFET. , 2020, , .		0

#	Article	IF	Citations
37	A 800MHz, 0.21pJ, 1.2V to 6V Level Shifter Using Thin Gate Oxide Devices in 65nm LSTP. , 2020, , .		0
38	A 585mV, 16.6fJ/cycle, 0.2Î¼W Variation Tolerant Scannable Hybrid Flip-Flop in 65nm CMOS LSTP. , 2021, , .		0