Tasleem Khan

List of Publications by Year
in descending order

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Version: 2024-02-01

13 papers	100 citations	1478505 6 h-index	1474206 9 g-index
13 all docs	13 docs citations	13 times ranked	57 citing authors

#	Article	IF	Citations
1	Optimal Complexity Architectures for Pipelined Distributed Arithmetic-Based LMS Adaptive Filter. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 630-642.	5.4	32
2	Low-Complexity Distributed-Arithmetic-Based Pipelined Architecture for an LSTM Network. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 329-338.	3.1	12
3	A Novel Time-Shared and LUT-Less Pipelined Architecture for LMS Adaptive Filter. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 188-197.	3.1	10
4	An Energy Efficient VLSI Architecture of Decision Feedback Equalizer for 5G Communication System. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2017, 7, 569-581.	3.6	8
5	Partial-LUT Designs for Low-Complexity Realization of DA-Based BLMS Adaptive Filter. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 1188-1192.	3.0	8
6	A New High Performance VLSI Architecture for LMS Adaptive Filter Using Distributed Arithmetic. , 2017, , .		7
7	Improved convergent distributed arithmetic based low complexity pipelined leastâ€meanâ€square filter. IET Circuits, Devices and Systems, 2018, 12, 792-801.	1.4	6
8	Low-Complexity Continuous-Flow Memory-Based FFT Architectures for Real-Valued Signals. , 2019, , .		5
9	High-Throughput and Improved-Convergent Design of Pipelined Adaptive DFE for 5G Communication. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 652-656.	3.0	3
10	An Efficient Scheme for Acoustic Echo Canceller Implementation Using Offset Binary Coding. IEEE Transactions on Instrumentation and Measurement, 2022, 71, 1-14.	4.7	3
11	High-Performance VLSI Architecture of DLMS Adaptive Filter for Fast-Convergence and Low-MSE. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 2106-2110.	3.0	3
12	Energy efficient VLSI architecture of realâ€valued serial pipelined FFT. IET Computers and Digital Techniques, 2019, 13, 461-469.	1.2	2
13	An Area and Power-Efficient Serial Commutator FFT with Recursive LUT Multiplier. Lecture Notes in Electrical Engineering, 2020, , 92-100.	0.4	1