Paul D Franzon

List of Publications by Citations

163 papers	2,134 citations	21 h-index	42 g-index
222 ext. papers	2,549 ext. citations	3.5 avg, IF	4.51 L-index

#	Paper	IF	Citations
163	FreePDK: An Open-Source Variation-Aware Design Kit **2007**,		200
162	An electronically tunable microstrip bandpass filter using thin-film Barium-Strontium-Titanate (BST) varactors. *IEEE Transactions on Microwave Theory and Techniques*, **2005**, 53, 2707-2712	4.1	179
161	An engineered virus as a scaffold for three-dimensional self-assembly on the nanoscale. *Small*, **2005**, 1, 702-6	11	105
160	Overview of RFID technology and its applications in the food industry. *Journal of Food Science*, **2009**, 74, R101-6	3.4	99
159	Controlled modulation of conductance in silicon devices by molecular monolayers. *Journal of the American Chemical Society*, **2006**, 128, 14537-41	16.4	98
158	. *IEEE Circuits and Systems Magazine*, **2012**, 12, 45-63	3.2	95
157	Nanocell logic gates for molecular computing. *IEEE Nanotechnology Magazine*, **2002**, 1, 100-109	2.6	91
156	NanoCell electronic memories. *Journal of the American Chemical Society*, **2003**, 125, 13279-83	16.4	90
155	A compact dielectric elastomer tubular actuator for refreshable Braille displays. *Sensors and Actuators A: Physical*, **2012**, 179, 151-157	3.9	78
154	Scaling constraints in nanoelectronic random-access memories. *Nanotechnology*, **2005**, 16, 2251-60	3.4	65
153	Configurable string matching hardware for speeding up intrusion detection. *Computer Architecture News*, **2005**, 33, 99-107		61
152	Through Silicon Via(TSV) defect/pinhole self test circuit for 3D-IC **2009**,		49
151	Load characterization of high displacement piezoelectric actuators with various end conditions. *Sensors and Actuators A: Physical*, **2001**, 94, 19-24	3.9	48
150	Controllable molecular modulation of conductivity in silicon-based devices. *Journal of the American Chemical Society*, **2009**, 131, 10023-30	16.4	46
149	Comparing Through-Silicon-Via (TSV) Void/Pinhole Defect Self-Test Methods. *Journal of Electronic Testing: Theory and Applications (JETTA)*, **2012**, 28, 27-38	0.7	42
148	. *IEEE Journal of Solid-State Circuits*, **1995**, 30, 571-579	5.5	42
147	Clustering effects on discontinuous gold film NanoCells. *Journal of Nanoscience and Nanotechnology*, **2004**, 4, 907-17	1.3	33

146	Design automation for a 3DIC FFT processor for synthetic aperture radar **2009**,		27
145	Accurate and Scalable IO Buffer Macromodel Based on Surrogate Modeling. *IEEE Transactions on Components, Packaging and Manufacturing Technology*, **2011**, 1, 1240-1249	1.7	24
144	. *IEEE Transactions on Advanced Packaging*, **2008**, 31, 711-721		23
143	Power comparison of 2D, 3D and 2.5D interconnect solutions and power optimization of interposer interconnects **2013**,		21
142	Surrogate-Model-Based Analysis of Analog Circuits—Part I: Variability Analysis. *IEEE Transactions on Device and Materials Reliability*, **2011**, 11, 458-465	1.6	21
141	Fundamental interconnection issues. *At&T Technical Journal*, **1987**, 66, 13-30		18
140	Surrogate-Model-Based Analysis of Analog Circuits—Part II: Reliability Analysis. *IEEE Transactions on Device and Materials Reliability*, **2011**, 11, 466-473	1.6	17
139	Fabrication of wafer scale, aligned sub-25nm nanowire and nanowire templates using planar edge defined alternate layer process. *Physica E: Low-Dimensional Systems and Nanostructures*, **2005**, 28, 107-114	3	17
138	. *IEEE Transactions on Semiconductor Manufacturing*, **1993**, 6, 77-82	2.6	17
137	AC coupled interconnect for dense 3-D ICs. *IEEE Transactions on Nuclear Science*, **2004**, 51, 2156-2160	1.7	15
136	. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2012**, 31, 676-689	2.5	14
135	Application Exploration for 3-D Integrated Circuits: TCAM, FIFO, and FFT Case Studies. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2009**, 17, 496-506	2.6	14
134	Electronic properties of molecular memory circuits on a nanoscale scaffold. *IEEE Transactions on Nanobioscience*, **2007**, 6, 270-4	3.4	13
133	Rationale for a 3D heterogeneous multi-core processor **2013**,		12
132	Creating 3D specific systems: Architecture, design and CAD **2010**,		11
131	Logic-on-logic 3D integration and placement **2010**,		11
130	. *IEEE/ASME Transactions on Mechatronics*, **2004**, 9, 392-398	5.5	11
129	. *IEEE Journal of Solid-State Circuits*, **1994**, 29, 1150-1153	5.5	11

128	Design and CAD for 3D integrated circuits **2008**,		10
127	A 36Gb/s ACCI Multi-Channel Bus using a Fully Differential Pulse Receiver **2006**,		10
126	. *IEEE Transactions on Smart Grid*, **2019**, 10, 714-721	10.7	10
125	. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2013**, 60, 1787-1799	3.9	9
124	A 32-Gb/s On-Chip Bus With Driver Pre-Emphasis Signaling. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2009**, 17, 1267-1274	2.6	9
123	Causal reduced-order modeling of distributed structures in a transient circuit Simulator. *IEEE Transactions on Microwave Theory and Techniques*, **2004**, 52, 2207-2214	4.1	9
122	Comparison of modeling techniques in circuit variability analysis. *International Journal of Numerical Modelling: Electronic Networks, Devices and Fields*, **2012**, 25, 288-302	1	8
121	Computing with Novel Floating-Gate Devices. *Computer*, **2011**, 44, 29-36	1.6	8
120	Multimode transceiver for high-density interconnects: Measurement and validation **2010**,		8
119	SOI CMOS Implementation of a Multirate PSK Demodulator for Space Communications. *IEEE Transactions on Circuits and Systems Part 1: Regular Papers*, **2007**, 54, 420-431		8
118	Reversible Modulation of Conductance in Silicon Devices via UV/Visible-Light Irradiation. *Advanced Materials*, **2008**, 20, 4541-4546	24	8
117	Flexible Low Power Probability Density Estimation Unit For Speech Recognition **2007**,		8
116	Machine learning in physical design **2016**,		8
115	Junction-level thermal extraction and simulation of 3DICs **2009**,		7
114	Multimode signaling on non-ideal channels **2008**,		7
113	Voltage-Mode Driver Preemphasis Technique For On-Chip Global Buses. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2007**, 15, 231-236	2.6	7
112	Fully Integrated AC Coupled Interconnect Using Buried Bumps. *IEEE Transactions on Advanced Packaging*, **2007**, 30, 191-199		7
111	Design Considerations and Benefits of Three-Dimensional Ternary Content Addressable Memory **2007**,		7

110	On Using the Volatile Mem-Capacitive Effect of TiO2 Resistive Random Access Memory to Mimic the Synaptic Forgetting Process. *Journal of Electronic Materials*, **2018**, 47, 994-997	1.9	7
109	A Transient Electrothermal Analysis of Three-Dimensional Integrated Circuits. *IEEE Transactions on Components, Packaging and Manufacturing Technology*, **2012**, 2, 660-667	1.7	6
108	Comparative analysis of two 3D integration implementations of a SAR processor **2009**,		6
107	Molectronics: a circuit design perspective **2001**, 4236, 80		6
106	Dynamic electrothermal simulation of three-dimensional integrated circuits using standard cell macromodels. *IET Circuits, Devices and Systems*, **2012**, 6, 35	1.1	6
105	Design of a rectifier-free UHF Gen-2 compatible RFID Tag using RF-only logic **2016**,		6
104	Thermal Pathfinding for 3-D ICs. *IEEE Transactions on Components, Packaging and Manufacturing Technology*, **2014**, 4, 1159-1168	1.7	5
103	Adaptive and Reliable Clock Distribution Design for 3-D Integrated Circuits. *IEEE Transactions on Components, Packaging and Manufacturing Technology*, **2014**, 4, 1862-1870	1.7	5
102	A 10.35 mW/GFlop stacked SAR DSP unit using fine-grain partitioned 3D integration **2012**,		5
101	Analog Negative-Bias-Temperature-Instability Monitoring Circuit. *IEEE Transactions on Device and Materials Reliability*, **2012**, 12, 177-179	1.6	5
100	Face-to-face bus design with built-in self-test in 3D ICs **2013**,		5
99	Application of surrogate modeling to generate compact and PVT-sensitive IBIS models **2009**,		5
98	A low power 3D integrated FFT engine using hypercube memory division **2009**,		5
97	Modeling and compare of through-silicon-via (TSV) in high frequency **2012**,		5
96	Physically based molecular device model in a transient circuit simulator. *Chemical Physics*, **2006**, 326, 188-196	2.3	5
95	Hardware Architecture of a Parallel Pattern Matching Engine **2007**,		5
94	. *IEEE Transactions on Components, Packaging and Manufacturing Technology*, **2015**, 5, 541-550	1.7	4
93	A Generally Applicable Calibration Algorithm for Digitally Reconfigurable Self-Healing RFICs. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2016**, 24, 1151-1164	2.6	4

92	Design of controller for L2 cache mapped in Tezzaron stacked DRAM **2013**,		4
91	Under 100-cycle thread migration latency in a single-ISA heterogeneous multi-core processor **2015**,		4
90	S-parameter based multimode signaling **2012**,		4
89	Hetero2 3D integration: A scheme for optimizing efficiency/cost of Chip Multiprocessors **2013**,		4
88	Reconfigurable five-layer three-dimensional integrated memory-on-logic synthetic aperture radar processor. *IET Computers and Digital Techniques*, **2011**, 5, 198	0.9	4
87	Adaptive clock distribution for 3D integrated circuits **2011**,		4
86	Pathfinder 3D: A flow for system-level design space exploration **2012**,		4
85	Design for 3D Integration and Applications **2007**,		4
84	. *IEEE Nanotechnology Magazine*, **2006**, 5, 356-361	2.6	4
83	Self-Evolution Cascade Deep Learning Model for High-Speed Receiver Adaptation. *IEEE Transactions on Components, Packaging and Manufacturing Technology*, **2020**, 10, 1043-1053	1.7	4
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81	. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2018**, 65, 406-418	3.9	3
80	Dual Floating Gate Unified Memory MOSFET With Simultaneous Dynamic and Non-Volatile Operation. *IEEE Electron Device Letters*, **2014**, 35, 48-50	4.4	3
79	Millimeter-Scale True 3-D Antenna-in-Package Structures for Near-Field Power Transfer. *IEEE Transactions on Components, Packaging and Manufacturing Technology*, **2014**, 4, 1574-1581	1.7	3
78	Parallel Transient Simulation of Multiphysics Circuits Using Delay-Based Partitioning. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2012**, 31, 1522-1535	2.5	3
77	Crosstalk-Canceling Multimode Interconnect Using Transmitter Encoding. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2013**, 21, 1562-1567	2.6	3
76	TSV-based, modular and collision detectable face-to-back shared bus design **2013**,		3
75	Thermal requirements in future 3D processors **2013**,		3

74	Inductively Coupled Connectors and Sockets for Multi-Gb/s Pulse Signaling. *IEEE Transactions on Advanced Packaging*, **2008**, 31, 749-758		3
73	AC coupled backplane communication using embedded capacitor **2008**,		3
72	Uniformity analysis of wafer scale sub-25nm wide nanowire array nanoimprint mold fabricated by PEDAL process. *Microelectronic Engineering*, **2007**, 84, 1523-1527	2.5	3
71	Architecture for Low Power Large Vocabulary Speech Recognition **2006**,		3
70	MEMS-based diffractive optical-beam-steering technology **1998**, 3276, 81		3
69	SABSA: SWITCHING-ACTIVITY-BASED STATE ASSIGNMENT. *International Journal of High Speed Electronics and Systems*, **1994**, 05, 203-212	0.5	3
68	Passive and Active Thermal Technologies: Modeling and Evaluation **2019**, 375-412		3
67	3D Stacked DRAM Memories **2019**, 149-186		2
66	Physical design of a 3D-stacked heterogeneous multi-core processor **2016**,		2
65	A Generic and Scalable Architecture for a Large Acoustic Model and Large Vocabulary Speech Recognition Accelerator Using Logic on Memory. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2014**, 22, 2701-2712	2.6	2
64	Pathfinder3D: A framework for exploring early thermal tradeoffs in 3DIC **2014**,		2
63	Exploring early design tradeoffs in 3DIC **2013**,		2
62	Circuit/channel co-design methodology for multimode signaling **2013**,		2
61	Computing in 3D **2015**,		2
60	Thermal simulation of heterogeneous GaN/ InP/silicon 3DIC stacks **2015**,		2
59	Process mismatch analysis based on reduced-order models **2012**,		2
58	**2012**,		2
57	Applications and design styles for 3DIC **2013**,		2

56	Low-Power Hypercube Divided Memory FFT Engine Using 3D Integration. *ACM Transactions on Design Automation of Electronic Systems*, **2010**, 16, 1-25	1.5	2
55	Thermal isolation in 3D chip stacks using vacuum gaps and capacitive or inductive communications **2010**,		2
54	A High K Nanocomposite for High Density Chip-to-Package Interconnections. *Materials Research Society Symposia Proceedings*, **2004**, 833, 185		2
53	A "defect level versus cost" system tradeoff for electronics manufacturing. *IEEE Transactions on Electronics Packaging Manufacturing*, **2004**, 27, 67-76		2
52	Driver pre-emphasis techniques for on-chip global buses **2005**,		2
51	Stochastic optimization approach to transistor sizing for CMOS VLSI circuits **1994**,		2
50	DeePar-SCA: Breaking Parallel Architectures of Lattice Cryptography via Learning Based Side-Channel Attacks. *Lecture Notes in Computer Science*, **2020**, 262-280	0.9	2
49	Hardware implementation of Hierarchical Temporal Memory algorithm **2016**,		2
48	RDL and interposer design for DiRAM4 interfaces **2016**,		2
47	Thermal raman and IR measurement of heterogeneous integration stacks **2016**,		2
46	. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2019**, 66, 756-768	3.9	2
45	An Application Specific Processor Architecture with 3D Integration for Recurrent Neural Networks **2019**,		1
44	Pre-Bond Testing Through Direct Probing of Large-Array Fine-Pitch Micro-Bumps* **2019**, 231-252		1
43	IEEE Std P1838: 3D Test Access Standard Under Development **2019**, 301-323		1
42	Thermal Isolation and Cooling Technologies for Heterogeneous 3D- and 2.5D-ICs **2019**, 347-373		1
41	Improved Numerical Methodologies on Power System Dynamic Simulation Using GPU Implementation **2019**,		1
40	A 0.65 mW/Gbps 30 Gbps capacitive coupled 10 mm serial link in 2.5D silicon interposer **2014**,		1
39	Near threshold RF-only analog to digital converter **2012**,		1

38	Surrogate Model-Based Self-Calibrated Design for Process and Temperature Compensation in Analog/RF Circuits. *IEEE Design and Test of Computers*, **2012**, 29, 74-83		1
37	Design, modeling, and fabrication of mm3 three-dimensional integrated antennas **2012**,		1
36	Analysis and approach of TSV-based hierarchical power distribution networks for estimating 1st-Droop and resonant noise in 3DIC **2011**,		1
35	SPICE-compatible physical model of nanocrystal floating gate devices for circuit simulation. *IET Circuits, Devices and Systems*, **2011**, 5, 477	1.1	1
34	Application of Quantum Machine Learning to VLSI Placement **2020**,		1
33	Multi-Fidelity Surrogate-Based Optimization for Electromagnetic Simulation Acceleration. *ACM Transactions on Design Automation of Electronic Systems*, **2020**, 25, 1-21	1.5	1
32	Design and Computer Aided Design of 3DIC. *Integrated Circuits and Systems*, **2011**, 75-88	0.2	1
31	. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2021**, 40, 1217-1229	2.5	1
30	Thermal Modeling and Model Validation for 3D Stacked ICs **2019**, 413-432		1
29	Design of a Rectifier-Free Near-Threshold UHF Gen2 RFID Tag using Dual-Phase RF-only Logic **2018**,		1
28	A Deep Transfer Learning Design Rule Checker with Synthetic Training. *IEEE Design and Test*, **2022**, 1-1	1.4	1
27	Multiphysics Challenges and Solutions for the Design of Heterogeneous 3D Integrated System **2019**, 53-79		0
26	Use of AC Coupled Interconnect in Contactless Packaging. *Integrated Circuits and Systems*, **2010**, 127-153	0.2	0
25	Exploring the Tradeoffs of Application-Specific Processing. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, **2018**, 8, 531-542	5.2	0
24	. *IEEE Journal of Radio Frequency Identification*, **2021**, 5, 317-323	2.4	0
23	Corrections to Crosstalk-Canceling Multimode Interconnect Using Transmitter Encoding[Aug 13 1562-1567]. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2017**, 25, 1792-1792	2.6	
22	3D Design Styles **2019**, 1-19		
21	Interconnect Testing for 2.5D- and 3D-SICs **2019**, 209-230		

20	3D Design-for-Test Architecture **2019**, 253-280	
19	Optimization of Test-Access Architectures and Test Scheduling for 3D ICs **2019**, 281-300	
18	Test and Debug Strategy for TSMC CoWoS Stacking Process-Based Heterogeneous 3D-IC: A Silicon Study **2019**, 325-346	
17	On the Thermal Management of 3D-ICs: From Backside to Volumetric Heat Removal **2019**, 433-460	
16	Ultrafine Pitch 3D Stacked Integrated Circuits: Technology, Design Enablement, and Application **2019**, 21-40	
15	Power Delivery Network and Integrity in 3D-IC Chips **2019**, 41-52	
14	Physical Design Flow for 3D/CoWoS Stacked ICs **2019**, 81-114	
13	Design and CAD Solutions for Cooling and Power Delivery for Monolithic 3D-ICs **2019**, 115-140	
12	Electronic Design Automation for 3D **2019**, 141-147	
11	Cost Modeling for 2.5D and 3D Stacked ICs **2019**, 187-208	
10	Asymmetric Transformer Design With Multiband Frequency Response for Simultaneous Power and Data Transfer. *IEEE Transactions on Components, Packaging and Manufacturing Technology*, **2020**, 10, 644-653	1.7
9	Model-Based Variation-Aware Integrated Circuit Design **2013**, 171-188	
8	Clocking Optimization and Distribution in Digital Systems with Scheduled Skews. *Journal of Signal Processing Systems*, **1997**, 16, 131-147	
7	Design for 3D Integration at North Carolina State University **2008**, 517-527	
6	Foreword Special Section on Electrical Performance Analysis and Simulation of Interconnects, Packages and Devices Composing Electronic Systems for High-Performance Applications. *IEEE Transactions on Advanced Packaging*, **2008**, 31, 662-663	
5	High Frequency, High Density Interconnect Using AC Coupling. *Materials Research Society Symposia Proceedings*, **2003**, 783, 611	
4	Hardware Implementation of Hierarchical Temporal Memory Algorithm. *ACM Journal on Emerging Technologies in Computing Systems*, **2022**, 18, 1-23	1.7
3	Variation-Aware Circuit Macromodeling and Design Based on Surrogate Models. *Advances in Intelligent Systems and Computing*, **2013**, 255-269	0.4

2	Simulation and Experimental Characterization of a Unified Memory Device with Two Floating-Gates. *IFIP Advances in Information and Communication Technology*, **2013**, 217-233	0.5
1	A Scalable Cluster-based Hierarchical Hardware Accelerator for a Cortically Inspired Algorithm. *ACM Journal on Emerging Technologies in Computing Systems*, **2021**, 17, 1-29	1.7