Partha Pande

List of Publications by Year
in descending order

Source: https://exaly.com/author-pdf/5234423/publications.pdf

Version: 2024-02-01

118 papers	3,666 citations	257357 24 h-index	155592 55 g-index
119 all docs	119 docs citations	119 times ranked	1686 citing authors

#	Article	IF	Citations
1	High-Throughput Training of Deep CNNs on ReRAM-Based Heterogeneous Architectures via Optimized Normalization Layers. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 1537-1549.	1.9	6
2	High-Performance and Energy-Efficient 3D Manycore GPU Architecture for Accelerating Graph Analytics. ACM Journal on Emerging Technologies in Computing Systems, 2022, 18, 1-19.	1.8	1
3	Special Issue on Near-Memory and In-Memory Processing. IEEE Design and Test, 2022, 39, 4-4.	1.1	0
4	Special Issue on Benchmarking Machine Learning Systems and Applications. IEEE Design and Test, 2022, 39, 4-4.	1.1	0
5	Special Issue on 2021 Top Picks in Hardware and Embedded Security. IEEE Design and Test, 2022, 39, 4-4.	1.1	0
6	NoC-enabled 3D Heterogeneous Manycore Systems for Big-Data Applications. , 2022, , .		0
7	AccuReD: High Accuracy Training of CNNs on ReRAM/GPU Heterogeneous 3-D Architecture. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 971-984.	1.9	28
8	HeM3D. ACM Transactions on Design Automation of Electronic Systems, 2021, 26, 1-21.	1.9	6
9	3D++: Unlocking the Next Generation of High-Performance and Energy-Efficient Architectures using M3D Integration. , 2021, , .		1
10	ReGraphX: NoC-enabled 3D Heterogeneous ReRAM Architecture for Training Graph Neural Networks. , 2021, , .		15
11	Power Management of Monolithic 3D Manycore Chips with Inter-tier Process Variations. ACM Journal on Emerging Technologies in Computing Systems, 2021, 17, 1-19.	1.8	3
12	Learning to Train CNNs on Faulty ReRAM-based Manycore Accelerators. Transactions on Embedded Computing Systems, 2021, 20, 1-23.	2.1	9
13	Performance and Accuracy Tradeoffs for Training Graph Neural Networks on ReRAM-Based Architectures. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021, 29, 1743-1756.	2.1	12
14	Learning Pareto-Frontier Resource Management Policies for Heterogeneous SoCs: An Information-Theoretic Approach. , 2021, , .		5
15	Heterogeneous Manycore Architectures Enabled by Processing-in-Memory for Deep Learning: From CNNs to GNNs: (ICCAD Special Session Paper). , 2021, , .		2
16	A General Hardware and Software Co-Design Framework for Energy-Efficient Edge AI. , 2021, , .		2
17	DARe: DropLayer-Aware Manycore ReRAM architecture for Training Graph Neural Networks. , 2021, , .		6
18	Multi-Objective Optimization of ReRAM Crossbars for Robust DNN Inferencing under Stochastic Noise. , 2021, , .		16

#	Article	IF	Citations
19	Inter-Tier Process-Variation-Aware Monolithic 3-D NoC Design Space Exploration. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 686-699.	2.1	9
20	A Hybrid 3D Interconnect With 2x Bandwidth Density Employing Orthogonal Simultaneous Bidirectional Signaling for 3D NoC. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 3919-3932.	3.5	7
21	3D-ReG. ACM Journal on Emerging Technologies in Computing Systems, 2020, 16, 1-24.	1.8	14
22	An Energy-aware Online Learning Framework for Resource Management in Heterogeneous Platforms. ACM Transactions on Design Automation of Electronic Systems, 2020, 25, 1-26.	1.9	20
23	Making a Case for Partially Connected 3D NoC. ACM Journal on Emerging Technologies in Computing Systems, 2020, 16, 1-17.	1.8	6
24	SETGAN. , 2020, , .		2
25	Analysis and Design Method of Multiple-Output Switched-Capacitor Voltage Regulators With a Reduced Number of Power Electronic Components. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 3234-3247.	3.5	5
26	A Dual-Output Step-Down Switched-Capacitor Voltage Regulator With a Flying Capacitor Crossing Technique for Enhanced Power Efficiency. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 2861-2871.	2.1	7
27	Dynamic Resource Management of Heterogeneous Mobile Platforms via Imitation Learning. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 2842-2854.	2.1	39
28	NoC-enabled software/hardware co-design framework for accelerating k-mer counting. , 2019, , .		8
29	MOOS. Transactions on Embedded Computing Systems, 2019, 18, 1-23.	2.1	22
30	REGENT: A Heterogeneous ReRAM/GPU-based Architecture Enabled by NoC for Training CNNs. , 2019, , .		13
31	A Machine Learning Framework for Multi-Objective Design Space Exploration and Optimization of Manycore Systems. , 2019, , .		1
32	Learning-Based Application-Agnostic 3D NoC Design for Heterogeneous Manycore Systems. IEEE Transactions on Computers, 2019, 68, 852-866.	2.4	47
33	A 40% PAE Frequency-Reconfigurable CMOS Power Amplifier With Tunable Gateâ€“Drain Neutralization for 28-GHz 5G Radios. IEEE Transactions on Microwave Theory and Techniques, 2018, 66, 2231-2245.	2.9	55
34	Zero-Power Feed-Forward Spur Cancelation for Supply-Regulated CMOS Ring PLLs. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 653-662.	2.1	5
35	On-Chip Communication Network for Efficient Training of Deep Convolutional Networks on Heterogeneous Manycore Systems. IEEE Transactions on Computers, 2018, 67, 672-686.	2.4	64
36	Hybrid on-chip communication architectures for heterogeneous manycore systems. , 2018, , .		4

#	Article	IF	Citations
37	Machine learning for design space exploration and optimization of manycore systems. , 2018, , .		28
38	Design Space Exploration of 3D Network-on-Chip. ACM Journal on Emerging Technologies in Computing Systems, 2018, 14, 1-26.	1.8	3
39	High-Performance and Small-Form Factor Near-Field Inductive Coupling for 3-D NoC. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 2921-2934.	2.1	9
40	A Spatial Multi-Bit Sub-1-V Time-Domain Matrix Multiplier Interface for Approximate Computing in 65-nm CMOS. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2018, 8, 506-518.	2.7	11
41	A 16-Gb/s Low-Power Inductorless Wideband Gain-Boosted Baseband Amplifier With Skewed Differential Topology for Wireless Network-on-Chip. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 2406-2418.	2.1	9
42	Trading-Off Accuracy and Energy of Deep Inference on Embedded Systems: A Co-Design Approach. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 2881-2893.	1.9	23
43	Machine Learning and Manycore Systems Design: A Serendipitous Symbiosis. Computer, 2018, 51, 66-77.	1.2	54
44	Scalable Network-on-Chip Architectures for Brainâ€“Machine Interface Applications. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 1895-1907.	2.1	5
45	Performance evaluation and design trade-offs for wireless-enabled SMART NoC. , 2017, , .		1
46	Switched Substrate-Shield-Based Low-Loss CMOS Inductors for Wide Tuning Range VCOs. IEEE Transactions on Microwave Theory and Techniques, 2017, 65, 2964-2976.	2.9	45
47	A Reconfigurable Wireless NoC for Large Scale Microbiome Community Analysis. IEEE Transactions on Computers, 2017, 66, 1653-1666.	2.4	6
48	Robust TSV-based 3D NoC design to counteract electromigration and crosstalk noise. , 2017, , .		6
49	Imitation Learning for Dynamic VFI Control in Large-Scale Manycore Systems. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 2458-2471.	2.1	44
50	Fully Integrated Buck Converter With Fourth-Order Low-Pass Filter. IEEE Transactions on Power Electronics, 2017, 32, 3700-3707.	5.4	24
51	Enabling High-Performance SMART NoC Architectures Using On-Chip Wireless Links. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 3495-3508.	2.1	12
52	3D NoC-Enabled Heterogeneous Manycore Architectures for Accelerating CNN Training. , 2017, , .		13
53	Energy and Area Efficient Near Field Inductive Coupling. , 2017, , .		10
54	Design-Space Exploration and Optimization of an Energy-Efficient and Reliable 3-D Small-World Network-on-Chip. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 719-732.	1.9	56

#	Article	IF	Citations
55	Multicast-Aware High-Performance Wireless Network-on-Chip Architectures. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 1126-1139.	2.1	46
56	Data analytics enables energy-efficiency and robustness. , 2017, , .		3
57	Energy-efficient and robust 3D NoCs with contactless vertical links (Invited paper). , 2017, , .		3
58	A dynamic, compiler guided DVFS mechanism to achieve energy-efficiency in multi-core processors. Sustainable Computing: Informatics and Systems, 2016, 12, 1-9.	1.6	7
59	High-Performance and Energy-Efficient Network-on-Chip Architectures for Graph Analytics. Transactions on Embedded Computing Systems, 2016, 15, 1-26.	2.1	16
60	Energy-efficient and reliable 3D network-on-chip (NoC): architectures and optimization algorithms. , 2016, , .		7
61	Optimization of dynamic power consumption in multi-tier gate-level monolithic 3D ICs. , 2016, , .		3
62	Network-on-Chip-Enabled Multicore Platforms for Parallel Model Predictive Control. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 2837-2850.	2.1	10
63	Wireless NoC and Dynamic VFI Codesign: Energy Efficiency Without Performance Penalty. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 2488-2501.	2.1	34
64	On-Chip Network-Enabled Many-Core Architectures for Computational Biology Applications. , 2015, , .		2
65	Introduction to IEEE Transactions on Multiscale Computing Systems (TMSCS). IEEE Transactions on Multi-Scale Computing Systems, 2015, 1, 2-6.	2.5	3
66	Optimizing 3D NoC design for energy efficiency: A machine learning approach. , 2015, , .		35
67	Improving EDP in wireless NoC-enabled multicore chips via DVFS pruning. , 2015, , .		0
68	An 18.7-Gb/s 60-GHz OOK Demodulator in 65-nm CMOS for Wireless Network-on-Chip. IEEE Transactions on Circuits and Systems I: Regular Papers, 2015, 62, 799-806.	3.5	49
69	DVFS Pruning for Wireless NoC Architectures. IEEE Design and Test, 2015, 32, 29-38.	1.1	15
70	Enhancing performance of wireless NoCs with distributed MAC protocols. , 2015, , .		18
71	Performance evaluation of wireless NoCs in presence of irregular network routing strategies. , 2014, , .		6
72	Hardware Accelerators in Computational Biology: Application, Potential, and Challenges. IEEE Design and Test, 2014, 31, 8-18.	1.1	8

#	Article	IF	Citations
73	Design Methodology for Optical Interconnect Topologies in NoCs With BER and Transmit Power Constraints. Journal of Lightwave Technology, 2014, 32, 163-175.	2.7	13
74	Wireless NoC Platforms With Dynamic Task Allocation for Maximum Likelihood Phylogeny Reconstruction. IEEE Design and Test, 2014, 31, 54-64.	1.1	4
75	A 1.2-pJ/bit 16-Gb/s 60-GHz OOK Transmitter in 65-nm CMOS for Wireless Network-On-Chip. IEEE Transactions on Microwave Theory and Techniques, 2014, 62, 2357-2369.	2.9	73
76	Thermal hotspot reduction in mm-Wave wireless NoC architectures. , 2014, , .		5
77	Architecture and Design of Multichannel Millimeter-Wave Wireless NoC. IEEE Design and Test, 2014, 31, 19-28.	1.1	73
78	Performance evaluation of wireless NoCs in presence of irregular network routing strategies. , 2014, , .		2
79	Design space exploration for reliable mm-wave wireless NoC architectures. , 2013, , .		9
80	A V-band wide locking-range injection-locked CMOS VCO for wireless network-on-chip receiver. , 2013, , .		2
81	Network-on-Chip with Long-Range Wireless Links for High-Throughput Scientific Computation. , 2013, , .		2
82	Evaluating effects of thermal management in wireless NoC-enabled multicore architectures. , 2013, , .		2
83	Sustainable dual-level DVFS-enabled NoC with on-chip wireless links. , 2013, , .		5
84	Design of an Energy-Efficient CMOS-Compatible NoC Architecture with Millimeter-Wave Wireless Interconnects. IEEE Transactions on Computers, 2013, 62, 2382-2396.	2.4	167
85	High-throughput, energy-efficient network-on-chip-based hardware accelerators. Sustainable Computing: Informatics and Systems, 2013, 3, 36-46.	1.6	8
86	Sustainable DVFS-Enabled Multi-Core Architectures with On-Chip Wireless Links. Advances in Computers, 2013, 88, 125-158.	1.2	2
87	Test Technology TC Newsletter. IEEE Design and Test of Computers, 2012, 29, 103-104.	1.4	0
88	Test Technology TC Newsletter. IEEE Design and Test of Computers, 2012, 29, 76-77.	1.4	0
89	On-Chip Network-Enabled Multicore Platforms Targeting Maximum Likelihood Phylogeny Reconstruction. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2012, 31, 1061-1073.	1.9	9
90	DVFS-enabled sustainable wireless NoC architecture. , 2012, , .		8

#	Article	IF	Citations
91	Wireless NoC as Interconnection Backbone for Multicore Chips: Promises and Challenges. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2012, 2, 228-239.	2.7	237
92	Test Technology TC Newsletter. IEEE Design and Test of Computers, 2012, 29, 107-108.	1.4	0
93	NoC-Based Hardware Accelerator for Breakpoint Phylogeny. IEEE Transactions on Computers, 2012, 61, 857-869.	2.4	12
94	Accelerating Maximum Likelihood Based Phylogenetic Kernels Using Network-on-Chip. , 2011, , .		4
95	A Unified Error Control Coding Scheme to Enhance the Reliability of a Hybrid Wireless Network-on-Chip. , 2011, , .		22
96	A wideband body-enabled millimeter-wave transceiver for wireless Network-on-Chip. , 2011, , .		37
97	Scalable Hybrid Wireless Network-on-Chip Architectures for Multicore Systems. IEEE Transactions on Computers, 2011, 60, 1485-1502.	2.4	229
98	Hardware accelerators for biocomputing: A survey. , 2010, , .		27
99	Network-on-Chip Hardware Accelerators for Biological Sequence Alignment. IEEE Transactions on Computers, 2010, 59, 29-41.	2.4	41
100	An optimized NoC architecture for accelerating TSP kernels in breakpoint median problem. , 2010, , .		2
101	Enhancing performance of network-on-chip architectures with millimeter-wave wireless interconnects. , 2010, , .		61
102	Comparative performance evaluation of wireless and optical NoC architectures. , 2010, , .		12
103	Performance evaluation of wireless networks on chip architectures. , 2009, , .		16
104	Networks-on-Chip in a Three-Dimensional Environment: A Performance Evaluation. IEEE Transactions on Computers, 2009, 58, 32-45.	2.4	394
105	Crosstalk-Aware Channel Coding Schemes for Energy Efficient and Reliable NOC Interconnects. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2009, 17, 1626-1639.	2.1	101
106	Design of Low Power & Reliable Networks on Chip Through Joint Crosstalk Avoidance and Multiple Error Correction Coding. Journal of Electronic Testing: Theory and Applications (JETTA), 2008, 24, 67-81.	0.9	40
107	Energy reduction through crosstalk avoidance coding in networks on chip. Journal of Systems Architecture, 2008, 54, 441-451.	2.5	18
108	Novel interconnect infrastructures for massive multicore chips â€" an overview. , 2008, , .		2

#	Article	IF	Citations
109	Addressing Signal Integrity in Networks on Chip Interconnects through Crosstalk-Aware Double Error Correction Coding. , 2007, , .		18
110	Performance Evaluation for Three-Dimensional Networks-On-Chip. , 2007, , .		55
111	Applicability of Energy Efficient Coding Methodology to Address Signal Integrity in 3D NoC Fabrics. , 2007, , .		4
112	Performance Evaluation of Adaptive Routing Algorithms for achieving Fault Tolerance in NoC Fabrics. , 2007, , .		39
113	NoC Interconnect Yield Improvement Using Crosspoint Redundancy. Defect and Fault Tolerance in VLSI Systems, Proceedings of the IEEE International Symposium on, 2006, , .	0.0	25
114	Design of Low power & Reliable Networks on Chip through joint crosstalk avoidance and forward error correction coding. Defect and Fault Tolerance in VLSI Systems, Proceedings of the IEEE International Symposium on, 2006, , .	0.0	41
115	Crosstalk-aware Energy Reduction in NoC Communication Fabrics. , 2006, , .		9
116	Timing analysis of network on chip architectures for MP-SoC platforms. Microelectronics Journal, 2005, 36, 833-845.	1.1	45
117	Performance Evaluation and Design Trade-Offs for Network-on-Chip Interconnect Architectures. IEEE Transactions on Computers, 2005, 54, 1025-1040.	2.4	678
118	On-line Fault Detection and Location for NoC Interconnects. , 0, , .		49