Esteban J GarzÃ³n C

List of Publications by Year
in descending order

28	231	933447 10	1058476 14
papers	citations	h-index	g-index

29	29	29	68
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Assessment of STT-MRAM performance at nanoscaled technology nodes using a device-to-memory simulation framework. Microelectronic Engineering, 2019, 215, 111009.	2.4	24
2	Assessment of STT-MRAMs based on double-barrier MTJs for cache applications by means of a device-to-system level simulation framework. The Integration VLSI Journal, 2020, 71, 56-69.	2.1	22
3	Exploiting STT-MRAMs for Cryogenic Non-Volatile Cache Applications. IEEE Nanotechnology Magazine, 2021, 20, 123-128.	2.0	21
4	Simulation Analysis of DMTJ-Based STT-MRAM Operating at Cryogenic Temperatures. IEEE Transactions on Magnetics, 2021, 57, 1-6.	2.1	16
5	Gain-Cell Embedded DRAM Under Cryogenic Operationâ€"A First Study. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021, 29, 1319-1324.	3.1	16
6	Hamming Distance Tolerant Content-Addressable Memory (HD-CAM) for DNA Classification. IEEE Access, 2022, 10, 28080-28093.	4.2	16
7	Ultralow Voltage FinFET- Versus TFET-Based STT-MRAM Cells for IoT Applications. Electronics (Switzerland), 2021, 10, 1756.	3.1	14
8	Reconfigurable CMOS/STT-MTJ Non-Volatile Circuit for Logic-in-Memory Applications. , 2020, , .		13
9	EDAM. , 2022, , .		13
10	A 0.05 mmÂ², 350 mV, 14 nW Fully-Integrated Temperature Sensor in 180-nm CMOS. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 749-753.	3.0	12
11	Relaxing non-volatility for energy-efficient DMTJ based cryogenic STT-MRAM. Solid-State Electronics, 2021, 184, 108090.	1.4	12
12	Embedded Memories for Cryogenic Applications. Electronics (Switzerland), 2022, 11, 61.	3.1	11
13	AIDA: Associative In-Memory Deep Learning Accelerator. IEEE Micro, 2022, 42, 67-75.	1.8	10
14	Exploiting Double-Barrier MTJs for Energy-Efficient Nanoscaled STT-MRAMs. , 2019, , .		6
15	Energy Efficient Self-Adaptive Dual Mode Logic Address Decoder. Electronics (Switzerland), 2021, 10, 1052.	3.1	5
16	Field-Free Magnetic Tunnel Junction for Logic Operations Based on Voltage-Controlled Magnetic Anisotropy. IEEE Magnetics Letters, 2021, 12, 1-4.	1.1	4
17	A 0.6Vâ€"1.8V Compact Temperature Sensor With 0.24 Â°C Resolution, Â±1.4 Â°C Inaccuracy and 1.06nJ per Conversion. IEEE Sensors Journal, 2022, 22, 11480-11488.	4.7	4
18	Remote control of VNA and parameter analyzer for RFCV measurements using Python. , 2016, , .		2

#	Article	IF	Citations
19	Space-time diversity for NLOS mitigation in TDOA-based positioning systems. , 2016, , .		2
20	Performance Benchmarking of TFET and FinFET Digital Circuits from a Synthesis-Based Perspective. Electronics (Switzerland), 2022, 11, 632.	3.1	2
21	Adjusting thermal stability in double-barrier MTJ for energy improvement in cryogenic STT-MRAMs. Solid-State Electronics, 2022, 194, 108315.	1.4	2
22	Fast computation of Cramer-Rao Bounds for TOA. , 2016, , .		1
23	Device-to-System Level Simulation Framework for STT-DMTJ Based Cache Memory. , 2019, , .		1
24	Voltage and Technology Scaling of DMTJ-based STT-MRAMs for Energy-Efficient Embedded Memories. , 2022, , .		1
25	Capacitance Extraction of 34-nm Metallurgical Channel Length MOSFET for Parasitic Assessment Using the RFCV Technique. , 2018, , .		0
26	Microprocessor Design with a Direct Bluetooth Connection in 45 nm Technology Using Microwind. , 2019, , .		0
27	Evaluating the Energy Efficiency of STT-MRAMs Based on Perpendicular MTJs with Double Reference Layers. , 2019, , .		0
28	Quantum capacitance transient phenomena in high-k dielectric armchair graphene nanoribbon field-effect transistor model. Solid-State Electronics, 2021, 184, 108060.	1.4	0