Swarup Bhunia

List of Publications by Year
in descending order

127	4,081	304743	175258
papers	citations	22 h-index	52 g-index

128	128	128	1927
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Pasteables: A Flexible and Smart "Stick-and-Peel" Wearable Platform for Fitness & Athletics. IEEE Consumer Electronics Magazine, 2024, , 1-1.	2.3	6
2	An Automated Framework for Board-Level Trojan Benchmarking. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2023, 42, 397-410.	2.7	1
3	LeGO: A Learning-Guided Obfuscation Framework for Hardware IP Protection. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 854-867.	2.7	10
4	BINGO: brain-inspired learning memory. Neural Computing and Applications, 2022, 34, 3223-3247.	5.6	2
5	HASTE: Software Security Analysis for Timing Attacks on Clear Hardware Assumption. IEEE Embedded Systems Letters, 2022, 14, 71-74.	1.9	4
6	A Wearable Skin Temperature Monitoring System for Early Detection of Infections. IEEE Sensors Journal, 2022, 22, 1670-1679.	4.7	10
7	Golden-Free Hardware Trojan Detection Using Self-Referencing. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2022, 30, 325-338.	3.1	6
8	ARTS: A Framework for AI-Rooted IoT System Design Automation. IEEE Embedded Systems Letters, 2022, 14, 151-154.	1.9	7
9	Addressing the range anxiety of battery electric vehicles with charging en route. Scientific Reports, 2022, 12, 5588.	3.3	44
10	SoCCom: Automated Synthesis of System-on-Chip Architectures. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2022, 30, 449-462.	3.1	2
11	SAIL: Analyzing Structural Artifacts of Logic Locking Using Machine Learning. IEEE Transactions on Information Forensics and Security, 2021, 16, 3828-3842.	6.9	11
12	CASTLE: Architecting Assured System-on-Chip Firmware Integrity. , 2021, , .		0
13	MAGIC: Machine-Learning-Guided Image Compression for Vision Applications in Internet of Things. IEEE Internet of Things Journal, 2021, 8, 7303-7315.	8.7	9
14	The Curious Case of Trusted IC Provisioning in Untrusted Testing Facilities. , 2021, , .		0
15	An Overview of Hardware Security and Trust: Threats, Countermeasures, and Design Tools. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 1010-1038.	2.7	56
16	NQR sensitive embedded signatures for authenticating additively manufactured objects. Scientific Reports, 2021, 11, 12207.	3.3	3
17	SILVerIn: Systematic Integrity Verification of Printed Circuit Board Using JTAG Infrastructure. ACM Journal on Emerging Technologies in Computing Systems, 2021, 17, 1-28.	2.3	4
18	SCOPE: Synthesis-Based Constant Propagation Attack on Logic Locking. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021, 29, 1529-1542.	3.1	24

#	Article	IF	Citations
19	Detecting Dye-Contaminated Vegetables Using Low-Field NMR Relaxometry. Foods, 2021, 10, 2232.	4.3	12
20	FaultDroid. ACM Transactions on Design Automation of Electronic Systems, 2021, 26, 1-27.	2.6	2
21	SARO: Scalable Attack-Resistant Logic Locking. IEEE Transactions on Information Forensics and Security, 2021, 16, 3724-3739.	6.9	9
22	On Database-Free Authentication of Microelectronic Components. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021, 29, 149-161.	3.1	5
23	A smart mask for active defense against airborne pathogens. Scientific Reports, 2021, 11, 19910.	3.3	13
24	SSEL: An Extensible Specification Language for SoC Security. , 2021, , .		0
25	SAFARI: Automatic Synthesis of Fault-Attack Resistant Block Cipher Implementations. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 752-765.	2.7	13
26	P2C2: Peer-to-Peer Car Charging. , 2020, , .		6
27	Clandestine nanoelectromechanical tags for identification and authentication. Microsystems and Nanoengineering, 2020, 6, 103.	7.0	4
28	Low Power Unsupervised Anomaly Detection by Nonparametric Modeling of Sensor Statistics. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 1833-1843.	3.1	14
29	Resilient System-on-Chip Designs With NoC Fabrics. IEEE Transactions on Information Forensics and Security, 2020, 15, 2808-2823.	6.9	8
30	Hardware Obfuscation and Logic Locking: A Tutorial Introduction. IEEE Design and Test, 2020, 37, 59-77.	1.2	7
31	Quality Obfuscation for Error-Tolerant and Adaptive Hardware IP Protection. , 2019, , .		8
32	SURF: Joint Structural Functional Attack on Logic Locking. , 2019, , .		29
33	An Intrinsic and Database-Free Authentication by Exploiting Process Variation in Back-End Capacitors. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 1253-1261.	3.1	4
34	Robust Authentication of Consumables With Extrinsic Tags and Chemical Fingerprinting. IEEE Access, 2019, 7, 14396-14409.	4.2	10
35	ReRAM-Based Intrinsically Secure Memory: A Feasibility Analysis. , 2019, , .		2
36	Sweep to the Secret: A Constant Propagation Attack on Logic Locking. , 2019, , .		32

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37	Guest Editorial: Special Section on Autonomous Intelligence for Security and Privacy Analytics. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 2703-2705.	3.1	0
38	Eat, but Verify: Low-Cost Portable Devices for Food Safety Analysis. IEEE Consumer Electronics Magazine, 2019, 8, 12-18.	2.3	8
39	System-on-chip security architecture and CAD framework for hardware patch. , 2018, , .		9
40	An automated configurable Trojan insertion framework for dynamic trust benchmarks. , 2018, , .		44
41	Hardware IP Trust Validation: Learn (the Untrustworthy), and Verify. , 2018, , .		32
42	Multi-Mode Micromechanical Resonant Tags for Traceability and Authentication Applications. , 2018, , .		1
43	SAIL: Machine Learning Guided Structural Analysis Attack on Hardware Obfuscation. , 2018, , .		81
44	Authentication of dietary supplements through Nuclear Quadrupole Resonance (NQR) spectroscopy. International Journal of Food Science and Technology, 2018, 53, 2796-2809.	2.7	4
45	Scalable Test Generation for Trojan Detection Using Side Channel Analysis. IEEE Transactions on Information Forensics and Security, 2018, 13, 2746-2760.	6.9	99
46	Development and Evaluation of Hardware Obfuscation Benchmarks. Journal of Hardware and Systems Security, 2018, 2, 142-161.	1.3	38
47	Security Assurance for System-on-Chip Designs With Untrusted IPs. IEEE Transactions on Information Forensics and Security, 2017, 12, 1515-1528.	6.9	50
48	Security vulnerability analysis of design-for-test exploits for asset protection in SoCs. , 2017, , .		29
49	A Uniquified Virtualization Approach to Hardware Security. IEEE Embedded Systems Letters, 2017, 9, 53-56.	1.9	7
50	Benchmarking of Hardware Trojans and Maliciously Affected Circuits. Journal of Hardware and Systems Security, 2017, 1, 85-102.	1.3	191
51	Golden-Free Hardware Trojan Detection with High Sensitivity Under Process Noise. Journal of Electronic Testing: Theory and Applications (JETTA), 2017, 33, 107-124.	1.2	45
52	A solitary protection measure against scan chain, fault injection, and power analysis attacks on AES. , 2017, , .		2
53	Tunable and Lightweight On-Chip Event Detection for Implantable Bladder Pressure Monitoring Devices. IEEE Transactions on Biomedical Circuits and Systems, 2017, 11, 1303-1312.	4.0	11
54	Guest Editors Introduction: Security of Beyond CMOS Devices: Issues and Opportunities. IEEE Transactions on Emerging Topics in Computing, 2017, 5, 302-303.	4.6	0

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55	Patching the internet of things. IEEE Spectrum, 2017, 54, 30-35.	0.7	17
56	A Security Perspective on Battery Systems of the Internet of Things. Journal of Hardware and Systems Security, 2017, 1, 188-199.	1.3	47
57	Editorial for the Introductory Issue of the Journal of Hardware and Systems Security (HaSS). Journal of Hardware and Systems Security, 2017, 1, 1-2.	1.3	0
58	Authentication and traceability of food products through the supply chain using NQR spectroscopy. , 2017, , .		7
59	Interleaved logic-in-memory architecture for energy-efficient fine-grained data processing. , 2017, , .		5
60	Energy-Efficient Reconfigurable Hardware Accelerators for Data-Intensive Applications. Journal of Low Power Electronics, 2017, 13, 382-394.	0.6	0
61	MERS. , 2016, , .		76
62	Wearables, Implants, and Internet of Things: The Technology Needs in the Evolving Landscape. IEEE Transactions on Multi-Scale Computing Systems, 2016, 2, 123-128.	2.4	16
63	Exploiting design-for-debug for flexible SoC security architecture. , 2016, , .		28
64	Security validation in IoT space. , 2016, , .		11
65	Energy-Efficient Adaptive Hardware Accelerator for Text Mining Application Kernels. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 3526-3537.	3.1	13
66	Design and Validation for FPGA Trust under Hardware Trojan Attacks. IEEE Transactions on Multi-Scale Computing Systems, 2016, 2, 186-198.	2.4	44
67	An Embedded Memory-Centric Reconfigurable Hardware Accelerator for Security Applications. IEEE Transactions on Computers, 2016, 65, 3196-3202.	3.4	3
68	SeMIA: Self-Similarity-Based IC Integrity Analysis. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, 35, 37-48.	2.7	31
69	DScanPUF: A Delay-Based Physical Unclonable Function Built Into Scan Chain. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 1059-1070.	3.1	25
70	Robust counterfeit PCB detection exploiting intrinsic trace impedance variations. , 2015, , .		33
71	A flexible architecture for systematic implementation of SoC security policies. , 2015, , .		40
72	Guest Editorsâ€™ Introduction: Wearables, Implants, and Internet of Things. IEEE Transactions on Multi-Scale Computing Systems, 2015, 1, 60-61.	2.4	1

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73	Guest Editorial Computing in Emerging Technologies (Second Issue). IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2015, 5, 1-4.	3.6	2
74	Silicon Carbide (SiC) Nanoelectromechanical Antifuse for Ultralow-Power One-Time-Programmable (OTP) FPGA Interconnects. IEEE Journal of the Electron Devices Society, 2015, 3, 323-335.	2.1	13
75	A Memory-Based Logic Block With Optimized-for-Read SRAM for Energy-Efficient Reconfigurable Computing Fabric. IEEE Transactions on Circuits and Systems II: Express Briefs, 2015, 62, 593-597.	3.0	8
76	Exploring Spin Transfer Torque Devices for Unconventional Computing. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2015, 5, 5-16.	3.6	17
77	Toward ultralow-power computing at exteme with silicon carbide (SiC) nanoelectromechanical logic. , 2014, , .		0
78	Implantable Ultrasonic Imaging Assembly for Automated Monitoring of Internal Organs. IEEE Transactions on Biomedical Circuits and Systems, 2014, 8, 881-890.	4.0	11
79	Hardware Trojan Attacks: Threat Analysis and Countermeasures. Proceedings of the IEEE, 2014, 102, 1229-1247.	21.3	534
80	Improving Energy Efficiency in FPGA Through Judicious Mapping of Computation to Embedded Memory Blocks. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 1314-1327.	3.1	10
81	VL-ECC: Variable Data-Length Error Correction Code for Embedded Memory in DSP Applications. IEEE Transactions on Circuits and Systems II: Express Briefs, 2014, 61, 120-124.	3.0	16
82	Toward ultralow-power computing at exteme with silicon carbide (SiC) nanoelectromechanical logic. , 2014, , .		1
83	Guest Editorial Computing in Emerging Technologies (First Issue). IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2014, 4, 377-379.	3.6	0
84	Hardware Trojan Detection by Multiple-Parameter Side-Channel Analysis. IEEE Transactions on Computers, 2013, 62, 2183-2195.	3.4	193
85	Protection Against Hardware Trojan Attacks: Towards a Comprehensive Solution. IEEE Design and Test, 2013, 30, 6-17.	1.2	99
86	A wearable ultrasonic assembly for point-of-care autonomous diagnostics of malignant growth. , 2013, , .		9
87	Ultralow-Power and Robust Embedded Memory for Bioimplantable Microsystems. , 2013, , .		2
88	Role of power grid in side channel attack and power-grid-aware secure design. , 2013, , .		38
89	Nanomechanical non-volatile memory for computing at extreme. , 2013, , .		5
90	SELF-HEALING DESIGN IN DEEP SCALED CMOS TECHNOLOGIES. Journal of Circuits, Systems and Computers, 2012, 21, 1240011.	1.5	2

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91	Width-Aware Fine-Grained Dynamic Supply Gating: A Design Methodology for Low-Power Datapath and Memory. , 2012, , .		1
92	SCARE: Side-Channel Analysis Based Reverse Engineering for Post-Silicon Validation. , 2012, , .		5
93	Healing of DSP Circuits Under Power Bound Using Post-Silicon Operand Bitwidth Truncation. IEEE Transactions on Circuits and Systems I: Regular Papers, 2012, 59, 1932-1941.	5.4	7
94	KiMS: Kids' Health Monitoring System at day-care centers using wearable sensors and vocabulary-based acoustic signal processing. , 2011, , .		15
95	VaROT: Methodology for Variation-Tolerant DSP Hardware Design Using Post-Silicon Truncation of Operand Width. , 2011, , .		7
96	NEMTronics: Symbiotic integration of nanoelectronic and nanomechanical devices for energy-efficient adaptive computing. , 2011, , .		1
97	Sequential hardware Trojan: Side-channel aware design and placement. , 2011, , .		34
98	Dynamic Transfer of Computation to Processor Cache for Yield and Reliability Improvement. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2011, 19, 1368-1379.	3.1	11
99	Reliability-Driven ECC Allocation for Multiple Bit Error Resilience in Processor Cache. IEEE Transactions on Computers, 2011, 60, 20-34.	3.4	50
100	Energy-Efficient Reconfigurable Computing Using a Circuit-Architecture-Software Co-Design Approach. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2011, 1, 369-380.	3.6	22
101	Ultra-Low-Power and Robust Digital-Signal-Processing Hardware for Implantable Neural Interface Microsystems. IEEE Transactions on Biomedical Circuits and Systems, 2011, 5, 169-178.	4.0	31
102	Security Against Hardware Trojan Attacks Using Key-Based Design Obfuscation. Journal of Electronic Testing: Theory and Applications (JETTA), 2011, 27, 767-785.	1.2	69
103	Multi-level attacks: An emerging security concern for cryptographic hardware. , 2011, , .		24
104	Electromechanical Computing at 500Â°C with Silicon Carbide. Science, 2010, 329, 1316-1318.	12.6	185
105	Digital signal processing in bio-implantable systems: Design challenges and emerging solutions. , 2010, , .		0
106	Security through obscurity: An approach for protecting Register Transfer Level hardware IP. , 2009, , .		27
107	Security against hardware Trojan through a novel application of design obfuscation. , 2009, , .		134
108	Hardware Trojan: Threats and emerging solutions. , 2009, , .		303

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109	Computing with nanoscale memory: Model and architecture. , 2009, , .		11
110	HARPOON: An Obfuscation-Based SoC Design Methodology for Hardware Protection. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2009, 28, 1493-1502.	2.7	376
111	Arbitrary Two-Pattern Delay Testing Using a Low-Overhead Supply Gating Technique. Journal of Electronic Testing: Theory and Applications (JETTA), 2008, 24, 577-590.	1.2	5
112	Within-Die Variation-Aware Scheduling in Superscalar Processors for Improved Throughput. IEEE Transactions on Computers, 2008, 57, 940-951.	3.4	15
113	Profit Aware Circuit Design Under Process Variations Considering Speed Binning. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2008, 16, 806-815.	3.1	20
114	On-demand transparency for improving hardware Trojan detectability. , 2008, , .		65
115	Hardware protection and authentication through netlist level obfuscation. , 2008, , .		102
116	Micropipeline-Based Asynchronous Design Methodology for Robust System Design Using Nanoscale Crossbar. , 2008, , .		0
117	Low-Overhead Circuit Synthesis for Temperature Adaptation Using Dynamic Voltage Scheduling. , 2007, , .		0
118	Memory based computation using embedded cache for processor yield and reliability improvement. , 2007, , .		1
119	Low-Power VLSI Architecture for Neural Data Compression Using Vocabulary-based Approach. , 2007, , .		7
120	Hybridization of CMOS With CNT-Based Nano-Electromechanical Switch for Low Leakage and Robust Circuit Design. IEEE Transactions on Circuits and Systems I: Regular Papers, 2007, 54, 2480-2488.	5.4	30
121	Ultralow-Power Reconfigurable Computing with Complementary Nano-Electromechanical Carbon Nanotube Switches. , 2007, , .		6
122	Vlm-Scan: A Low Overhead Scan Design Approach for Protection of Secret Key in Scan-Based Secure Chips. VLSI Test Symposium (VTS), Proceedings, IEEE, 2007, , .	1.0	85
123	Low-overhead design technique for calibration of maximum frequency at multiple operating points. IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, 2007, , .	0.0	3
124	Device-Aware Yield-Centric Dual-V_{t} Design Under Parameter Variations in Nanoscale Technologies. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2007, 15, 660-671.	3.1	14
125	A New Paradigm for Low-power, Variation-Tolerant Circuit Synthesis Using Critical Path Isolation. IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, 2006, , .	0.0	1
126	Defect Oriented Testing of Analog Circuits Using Wavelet Analysis of Dynamic Supply Current. Journal of Electronic Testing: Theory and Applications (JETTA), 2005, 21, 147-159.	1.2	18

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127	GAARP: A Power-Aware GALS Architecture for Real-Time Algorithm-Specific Tasks. IEEE Transactions on Computers, 2005, 54, 752-766.	3.4	11