Juin J Liou

List of Publications by Year
in descending order

164	2,010	304368	315357
papers	citations	22 h-index	38 g-index

166	166	166	1242
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Revisiting MOSFET threshold voltage extraction methods. Microelectronics Reliability, 2013, 53, 90-104.	0.9	220
2	RF transistors: Recent developments and roadmap toward terahertz applications. Solid-State Electronics, 2007, 51, 1079-1091.	0.8	107
3	A Review of Core Compact Models for Undoped Double-Gate SOI MOSFETs. IEEE Transactions on Electron Devices, 2007, 54, 131-140.	1.6	104
4	Novel Silicon-Controlled Rectifier (SCR) for High-Voltage Electrostatic Discharge (ESD) Applications. IEEE Electron Device Letters, 2008, 29, 753-755.	2.2	74
5	A New High Holding Voltage Dual-Direction SCR With Optimized Segmented Topology. IEEE Electron Device Letters, 2016, 37, 1311-1313.	2.2	59
6	Silicon-Controlled Rectifier Stacking Structure for High-Voltage ESD Protection Applications. IEEE Electron Device Letters, 2010, 31, 845-847.	2.2	56
7	An Improved Bidirectional SCR Structure for Low-Triggering ESD Protection Applications. IEEE Electron Device Letters, 2008, 29, 360-362.	2.2	54
8	RF MOSFET: recent advances, current status and future trends. Solid-State Electronics, 2003, 47, 1881-1895.	0.8	44
9	High-Robustness and Low-Capacitance Silicon-Controlled Rectifier for High-Speed I/O ESD Protection. IEEE Electron Device Letters, 2013, 34, 178-180.	2.2	40
10	A review of DC extraction methods for MOSFET series resistance and mobility degradation model parameters. Microelectronics Reliability, 2017, 69, 1-16.	0.9	38
11	An Explicit Surface Potential Calculation and Compact Current Model for AlGaN/GaN HEMTs. IEEE Electron Device Letters, 2015, 36, 108-110.	2.2	35
12	TCAD Methodology for Design of SCR Devices for Electrostatic Discharge (ESD) Applications. IEEE Transactions on Electron Devices, 2007, 54, 822-832.	1.6	34
13	Silicon-Controlled Rectifier for Electrostatic Discharge Protection Solutions With Minimal Snapback and Reduced Overshoot Voltage. IEEE Electron Device Letters, 2015, 36, 424-426.	2.2	33
14	Novel Capacitance Coupling Complementary Dual-Direction SCR for High-Voltage ESD. IEEE Electron Device Letters, 2012, 33, 640-642.	2.2	31
15	Growth of Tellurium Nanobelts on h-BN for p-type Transistors with Ultrahigh Hole Mobility. Nano-Micro Letters, 2022, 14, 109.	14.4	31
16	High-Holding-Voltage Silicon-Controlled Rectifier for ESD Applications. IEEE Electron Device Letters, 2012, 33, 1345-1347.	2.2	30
17	Investigation of LOCOS- and Polysilicon-Bound Diodes for Robust Electrostatic Discharge (ESD) Applications. IEEE Transactions on Electron Devices, 2010, 57, 814-819.	1.6	28
18	Bidirectional Devices for Automotive-Grade Electrostatic Discharge Applications. IEEE Electron Device Letters, 2012, 33, 860-862.	2.2	27

#	Article	IF	Citations
19	Bidirectional Diode-Triggered Silicon-Controlled Rectifiers for Low-Voltage ESD Protection. IEEE Electron Device Letters, 2012, 33, 1360-1362.	2.2	27
20	Design and Analysis of an Area-Efficient High Holding Voltage ESD Protection Device. IEEE Transactions on Electron Devices, 2015, 62, 606-614.	1.6	26
21	RC-Embedded LDMOS-SCR With High Holding Current for High-Voltage I/O ESD Protection. IEEE Transactions on Device and Materials Reliability, 2015, 15, 495-499.	1.5	26
22	Modelling solar cell S-shaped I-V characteristics with DC lumped-parameter equivalent circuits a review. Facta Universitatis - Series Electronics and Energetics, 2017, 30, 327-350.	0.6	24
23	Snapback and Postsnapback Saturation of Pseudomorphic High-Electron Mobility Transistor Subject to Transient Overstress. IEEE Electron Device Letters, 2010, 31, 425-427.	2.2	22
24	An Improved Compact Model of Silicon-Controlled Rectifier (SCR) for Electrostatic Discharge (ESD) Applications. IEEE Transactions on Electron Devices, 2008, 55, 3517-3524.	1.6	21
25	A New Analytical Subthreshold Potential/Current Model for Quadruple-Gate Junctionless MOSFETs. IEEE Transactions on Electron Devices, 2014, 61, 1972-1978.	1.6	21
26	An Unassisted, Low Trigger-, and High Holding-Voltage SCR (uSCR) for On-Chip ESD-Protection Applications. IEEE Electron Device Letters, 2007, 28, 1120-1122.	2.2	18
27	Indirect fitting procedure to separate the effects of mobility degradation and source-and-drain resistance in MOSFET parameter extraction. Microelectronics Reliability, 2009, 49, 689-692.	0.9	18
28	Analysis of Safe Operating Area of NLDMOS and PLDMOS Transistors Subject to Transient Stresses. IEEE Transactions on Electron Devices, 2010, 57, 2655-2663.	1.6	18
29	Status and Future Prospects of CMOS Scaling and Moore's Law - A Personal Perspective. , 2020, , .		18
30	Self-assembling SiC nanoflakes/MXenes composites embedded in polymers towards efficient electromagnetic wave attenuation. Applied Surface Science, 2022, 574, 151463.	3.1	18
31	Optimized pMOS-Triggered Bidirectional SCR for Low-Voltage ESD Protection Applications. IEEE Transactions on Electron Devices, 2014, 61, 2588-2594.	1.6	17
32	Compact Thermal Failure Model for Devices Subject to Electrostatic Discharge Stresses. IEEE Transactions on Electron Devices, 2015, 62, 4128-4134.	1.6	17
33	An analytical threshold voltage model of NMOSFETs with hot-carrier induced interface charge effect. Microelectronics Reliability, 2005, 45, 1144-1149.	0.9	16
34	A new model for four-terminal junction field-effect transistors. Solid-State Electronics, 2006, 50, 422-428.	0.8	16
35	Prediction and Modeling of Thin Gate Oxide Breakdown Subject to Arbitrary Transient Stresses. IEEE Transactions on Electron Devices, 2010, 57, 2296-2305.	1.6	16
36	An Enhanced MLSCR Structure Suitable for ESD Protection in Advanced Epitaxial CMOS Technology. IEEE Transactions on Electron Devices, 2019, 66, 2062-2067.	1.6	16

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37	Effects of anode materials on resistive characteristics of NiO thin films. Applied Physics Letters, 2013, 102, .	1.5	15
38	p-AlInN electron blocking layer for AlGaN-based deep-ultraviolet light-emitting diode. Superlattices and Microstructures, 2021, 158, 107022.	1.4	15
39	Evaluating MOSFET harmonic distortion by successive integration of the Iâ€“V characteristics. Solid-State Electronics, 2008, 52, 1092-1098.	0.8	14
40	Electrostatic Discharge Robustness of Si Nanowire Field-Effect Transistors. IEEE Electron Device Letters, 2009, 30, 969-971.	2.2	14
41	A Compact and Self-Isolated Dual-Directional Silicon Controlled Rectifier (SCR) for ESD Applications. IEEE Transactions on Device and Materials Reliability, 2019, 19, 169-175.	1.5	14
42	New Diode-Triggered Silicon-Controlled Rectifier for Robust Electrostatic Discharge Protection at High Temperatures. IEEE Transactions on Electron Devices, 2019, 66, 2044-2048.	1.6	14
43	A New Method to Estimate Failure Temperatures of Semiconductor Devices Under Electrostatic Discharge Stresses. IEEE Electron Device Letters, 2016, 37, 1477-1480.	2.2	13
44	Augmented DTSCR With Fast Turn-On Speed for Nanoscale ESD Protection Applications. IEEE Transactions on Electron Devices, 2020, 67, 1353-1356.	1.6	13
45	An Improved Silicon-Controlled Rectifier (SCR) for Low-Voltage ESD Application. IEEE Transactions on Electron Devices, 2020, 67, 576-581.	1.6	13
46	Gate oxide evaluation under very fast transmission line pulse (VFTLP) CDM-type stress. , 2008, , .		12
47	Development of a New pHEMT-Based Electrostatic Discharge Protection Structure. IEEE Transactions on Electron Devices, 2011, 58, 2974-2980.	1.6	12
48	Minimizing Multiple Triggering Effect in Diode-Triggered Silicon-Controlled Rectifiers for ESD Protection Applications. IEEE Electron Device Letters, 2012, 33, 893-895.	2.2	12
49	Study of Organic Thin-Film Transistors Under Electrostatic Discharge Stresses. IEEE Electron Device Letters, 2011, 32, 967-969.	2.2	11
50	No-Snapback Silicon-Controlled Rectifier for Electrostatic Discharge Protection of High-Voltage ICs. IEEE Electron Device Letters, 2015, 36, 1121-1123.	2.2	11
51	A double snapback SCR ESD protection scheme for 28â€¯nm CMOS process. Microelectronics Reliability, 2018, 84, 20-25.	0.9	11
52	Digital Volume Pulse Measured at the Fingertip as an Indicator of Diabetic Peripheral Neuropathy in the Aged and Diabetic. Entropy, 2019, 21, 1229.	1.1	11
53	An improved electrostatic discharge protection structure for reducing triggering voltage and parasitic capacitance. Solid-State Electronics, 2003, 47, 1105-1110.	0.8	10
54	Substrate current, gate current and lifetime prediction of deep-submicron nMOS devices. Solid-State Electronics, 2005, 49, 505-511.	0.8	10

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55	Robust ESD Protection Solutions in CMOS/BiCMOS Technologies. , 2007, , .		10
56	Failure Analysis of Si Nanowire Field-Effect Transistors Subject to Electrostatic Discharge Stresses. IEEE Electron Device Letters, 2010, 31, 915-917.	2.2	10
57	Development of an Electrostatic Discharge Protection Solution in GaN Technology. IEEE Electron Device Letters, 2013, 34, 1491-1493.	2.2	10
58	A unified look at the use of successive differentiation and integration in MOSFET model parameter extraction. Microelectronics Reliability, 2015, 55, 293-307.	0.9	10
59	Characteristics of ESD protection devices operated under elevated temperatures. Microelectronics Reliability, 2016, 66, 46-51.	0.9	10
60	ESD protection structure with reduced capacitance and overshoot voltage for high speed interface applications. Microelectronics Reliability, 2017, 79, 201-205.	0.9	10
61	An Enhanced Gate-Grounded NMOSFET for Robust ESD Applications. IEEE Electron Device Letters, 2019, 40, 1491-1494.	2.2	10
62	Determination of gate-bias dependent source/drain series resistance and effective channel length for advanced MOS devices. Solid-State Electronics, 2006, 50, 1774-1779.	0.8	9
63	On-chip electrostatic discharge protection for CMOS gas sensor systems-on-a-chip (SoC). Microelectronics Reliability, 2006, 46, 1285-1294.	0.9	9
64	A Novel Capacitance-Coupling-Triggered SCR for Low-Voltage ESD Protection Applications. IEEE Electron Device Letters, 2010, 31, 1089-1091.	2.2	9
65	A Reliable Si₃N₄/Al₂O₃-HfO₂Stack MIM Capacitor for High-Voltage Analog Applications. IEEE Transactions on Electron Devices, 2014, 61, 2944-2949.	1.6	9
66	ESD Protection Device With Dual-Polarity Conduction and High Blocking Voltage Realized in CMOS Process. IEEE Electron Device Letters, 2014, 35, 437-439.	2.2	9
67	Compact failure modeling for devices subject to electrostatic discharge stresses â€“ A review pertinent to CMOS reliability simulation. Microelectronics Reliability, 2015, 55, 15-23.	0.9	9
68	A surface-potential-based drain current compact model for a-InGaZnO thin-film transistors in Non-Degenerate conduction regime. Solid-State Electronics, 2017, 137, 38-43.	0.8	9
69	Nanoscale Bias-Annealing Effect in Postirradiated Thin Silicon Dioxide Films Observed by Conductive Atomic Force Microscopy. IEEE Transactions on Device and Materials Reliability, 2007, 7, 351-355.	1.5	8
70	Correlation of Human Metal Model and Transmission Line Pulsing Testing. IEEE Electron Device Letters, 2011, 32, 1200-1202.	2.2	8
71	Design and characterization of ESD solutions with EMC robustness for automotive applications. Microelectronics Reliability, 2015, 55, 2236-2246.	0.9	8
72	Bidirectional siliconâ€controlled rectifier for advanced ESD protection applications. Electronics Letters, 2019, 55, 112-114.	0.5	8

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73	Influence of polysilicon-gate depletion on the subthreshold behavior of submicron MOSFETs. Microelectronics Reliability, 2002, 42, 343-347.	0.9	7
74	Prediction of Gate Dielectric Breakdown in the CDM timescale utilizing very fast transmission line pulsing. , 2009, , .		7
75	Very small snapback silicon-controlled rectifier for electrostatic discharge protection in 28nm processing. Microelectronics Reliability, 2016, 61, 106-110.	0.9	7
76	A compact drain current model for heterostructure HEMTs including 2DEG density solution with two subbands. Solid-State Electronics, 2016, 115, 54-59.	0.8	7
77	Robust Protection Device for Electrostatic Discharge/Electromagnetic Interference in Industrial Interface Applications. IEEE Transactions on Device and Materials Reliability, 2016, 16, 263-265.	1.5	7
78	Relative Errors of Free-Carrier Density at Different Temperatures Calculated from Approximations for the Fermi-Dirac Integral. Japanese Journal of Applied Physics, 1995, 34, 2286-2287.	0.8	6
79	Investigation of diode geometry and metal line pattern for robust ESD protection applications. Microelectronics Reliability, 2008, 48, 1660-1663.	0.9	6
80	A new integration-based procedure to separately extract series resistance and mobility degradation in MOSFETs. Semiconductor Science and Technology, 2009, 24, 105015.	1.0	6
81	Integration-based approach to evaluate the sub-threshold slope of MOSFETs. Microelectronics Reliability, 2010, 50, 312-315.	0.9	6
82	Challenges of electrostatic discharge (ESD) protection in silicon nanowire technology. , 2012, , .		6
83	Compact and Low Leakage Devices for Bidirectional Low-Voltage ESD Protection Applications. IEEE Electron Device Letters, 2021, 42, 391-394.	2.2	6
84	Compositionally graded AlGaN hole source layer for deep-ultraviolet nanowire light-emitting diode without electron blocking layer. Nanotechnology, 2022, 33, 075205.	1.3	6
85	Statistical modeling of MOS devices for parametric yield prediction. Microelectronics Reliability, 2002, 42, 787-795.	0.9	5
86	Modeling of On-Chip Differential Inductors and Transformers/Baluns. IEEE Transactions on Electron Devices, 2007, 54, 369-371.	1.6	5
87	Evaluation of RF electrostatic discharge (ESD) protection in 0.18-Î¼m CMOS technology. Microelectronics Reliability, 2008, 48, 995-999.	0.9	5
88	Multiple-finger turn-on uniformity in silicon-controlled rectifiers. Solid-State Electronics, 2010, 54, 1641-1643.	0.8	5
89	Segmented SCR for high voltage ESD protection. , 2012, , .		5
90	NLDMOS ESD Scaling Under Human Metal Model for 40-V Mixed-Signal Applications. IEEE Electron Device Letters, 2012, 33, 1595-1597.	2.2	5

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91	A Physics-Based Compact Model for Symmetrical Double-Gate Polysilicon Thin-Film Transistors. IEEE Transactions on Electron Devices, 2017, 64, 2221-2227.	1.6	5
92	Effects of incomplete ionization of impurity dopants on the performance of bipolar junction transistors. Solid-State Electronics, 1996, 39, 318-320.	0.8	4
93	Optimization of on-chip ESD protection structures for minimal parasitic capacitance. Microelectronics Reliability, 2003, 43, 725-733.	0.9	4
94	An improved junction capacitance model for junction field-effect transistors. Solid-State Electronics, 2006, 50, 1395-1399.	0.8	4
95	InGaP/GaAs heterojunction bipolar transistor and RF power amplifier reliability. Microelectronics Reliability, 2008, 48, 1212-1215.	0.9	4
96	Low-Capacitance SCR Structure for RF I/O Application. IEEE Transactions on Electromagnetic Compatibility, 2013, 55, 241-247.	1.4	4
97	Application of multiscale PoincarÃ© short-time computation versus multiscale entropy in analyzing fingertip photoplethysmogram amplitudes to differentiate diabetic from non-diabetic subjects. Computer Methods and Programs in Biomedicine, 2018, 166, 115-121.	2.6	4
98	Low-power High-speed Dynamic Comparator Using a New Regenerative Stage. , 2018, , .		4
99	Reliability Issues of Thin Film Transistors Subject to Electrostatic Discharge Stresses: An Overview. Advanced Electronic Materials, 2022, 8, .	2.6	4
100	A Novel and Robust Un-Assisted, Low-Trigger and High-Holding Voltage SCR (uSCR) for Area-Efficient On-Chip ESD Protection. , 2007, , .		3
101	Silicon controlled rectifier (SCR) compact modeling based on VBIC and Gummelâ€“Poon models. Solid-State Electronics, 2009, 53, 195-203.	0.8	3
102	Thermal reliability of VCO using InGaP/GaAs HBTs. Microelectronics Reliability, 2011, 51, 2147-2152.	0.9	3
103	vfTLP-VTH: A new method for quantifying the effectiveness of ESD protection for the CDM classification test. Microelectronics Reliability, 2013, 53, 196-204.	0.9	3
104	Metal-Semiconductor-Insulator-Metal Structure Field-Effect Transistors Based on Zinc Oxides and Doped Ferroelectric Thin Films. Materials Research Society Symposia Proceedings, 2014, 1633, 131-137.	0.1	3
105	Reference voltage generation scheme enhancing speed and reliability for 1T1Câ€type FRAM. Electronics Letters, 2014, 50, 154-156.	0.5	3
106	Study on leakage current properties of BiFeO₃ thin films with Pb(Zr,Ti)O₃ buffer layer. Ferroelectrics, 2016, 504, 172-179.	0.3	3
107	Embedded shunt diode pair to suppress overshoot voltage. , 2017, , .		3
108	A Unified Quasi-3D Subthreshold Behavior Model for Multiple-Gate MOSFETs. IEEE Nanotechnology Magazine, 2018, , 1-1.	1.1	3

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109	Impact of the gate structure on ESD characteristic of tunnel field-effect transistors. , 2018, , .		3
110	Back-End-of-Line-Based Resistive RAM in 0.13 Î¼ m Partially-Depleted Silicon-on-Insulator Process for Highly Reliable Irradiation- Resistant Application. IEEE Electron Device Letters, 2021, 42, 30-33.	2.2	3
111	Improved LDMOSâ€SCR for highâ€voltage electrostatic discharge (ESD) protection applications. Electronics Letters, 2020, 56, 680-682.	0.5	3
112	Investigation and Suppression of Holding Voltage Deterioration in Multifinger SCR for Robust High-Voltage ESD Engineering. IEEE Transactions on Electron Devices, 2021, 68, 6338-6343.	1.6	3
113	Worst-case analysis and statistical simulation of MOSFET devices based on parametric test data. Solid-State Electronics, 2001, 45, 1537-1547.	0.8	2
114	Empirical reliability modeling for 0.18-Î¼m MOS devices. Solid-State Electronics, 2003, 47, 1515-1522.	0.8	2
115	Very fast transient simulation and measurement methodology for ESD technology development. Reliability Physics Symposium, 2009 IEEE International, 2009, , .	0.0	2
116	Extraction of MOSFET Model Parameters from the Measured Source-to-drain Resistance. ECS Transactions, 2009, 23, 353-360.	0.3	2
117	Evaluation of Transient Behavior of Polysilicon-Bound Diode for Fast ESD Applications. IEEE Transactions on Electron Devices, 2010, 57, 2736-2743.	1.6	2
118	Self-protection capability of integrated NLDMOS power arrays in ESD pulse regimes. Microelectronics Reliability, 2011, 51, 2015-2030.	0.9	2
119	In Situ ESD Protection Structure for Variable Operating Voltage Interface Applications in 28-nm CMOS Process. IEEE Transactions on Device and Materials Reliability, 2014, 14, 1061-1067.	1.5	2
120	A Novel Effective-Conducting-Path-Induced Scaling Length Model and Its Application for Assessing Short-Channel Performance of Multiple-Gate MOSFETs. IEEE Transactions on Electron Devices, 2018, 65, 4535-4541.	1.6	2
121	A Modified LDMOS-SCR with High Holding Voltage for high voltage ESD Protection. , 2019, , .		2
122	White Organic Light-emitting Diode Using Nano-double Ultrathin Carrier-trapping Materials in Performance Stability. Sensors and Materials, 2019, 31, 131.	0.3	2
123	A LVTSCR-Based Compact Structure for Latch-up Immune. , 2021, , .		2
124	Segmentation of breast tumors using cutting-edge semantic segmentation models. Computer Methods in Biomechanics and Biomedical Engineering: Imaging and Visualization, 2023, 11, 242-252.	1.3	2
125	Advanced ESD Protection Solutions in CMOS/BiCMOS Technologies. ECS Transactions, 2007, 9, 97-102.	0.3	1
126	Reliability study of ultrathin oxide films subject to irradiation-then-stress treatment using conductive atomic force microscopy. Microelectronics Reliability, 2007, 47, 419-421.	0.9	1

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127	Study of Electrothermal Stress Effect on RF Performance of InGaP/GaAs Heterojunction Bipolar Transistor-Based Low-Noise Amplifier. Compound Semiconductor Integrated Circuit Symposium (CSICS), IEEE, 2008, , .	0.0	1
128	Acomprehensive compact SCR model for CDM ESD circuit simulation. , 2008, , .		1
129	A fully on-chip ESD protection UWB-band low noise amplifier using GaAs enhancement-mode dual-gate pHEMT technology. Microelectronics Reliability, 2011, 51, 2137-2142.	0.9	1
130	Miscorrelation Between Air Gap Discharge and Human Metal Model Stresses Due to Multi-Finger Turn-On Effect. IEEE Transactions on Device and Materials Reliability, 2014, 14, 864-868.	1.5	1
131	A Novel Product-Level Human Metal Model Characterization Methodology. IEEE Transactions on Device and Materials Reliability, 2014, 14, 772-774.	1.5	1
132	Design optimization of SiGe BiCMOS Silicon Controlled Rectifier for Charged Device Model (CDM) protection applications. Microelectronics Reliability, 2014, 54, 57-63.	0.9	1
133	Investigation of forward transient characteristics of vertical GaN-on-GaN p-n diodes. , 2016, , .		1
134	Heterogeneous stacking silicon controlled rectifier design with improved ESD performance. , 2017, , .		1
135	Effect of P-type Guard ring on the Turn-on Characteristics of Diode-triggered SCR. , 2019, , .		1
136	Extended-gate Field Effect Transistors with Zinc Oxide as sensing film for pH Sensing. , 2021, , .		1
137	ESD Breakdown of Parylene OFETs With Varying Contact Overlap Capacitance. IEEE Transactions on Electron Devices, 2021, 68, 4630-4636.	1.6	1
138	A comprehensive and analytical drain current model for pocket-implanted NMOSFETs. Solid-State Electronics, 2004, 48, 327-333.	0.8	0
139	A novel low-trigger and high-holding voltage SCR without externally- assisted circuitry for area-efficient on-chip ESD protection. , 2007, , .		0
140	Electro-thermal stress effect on InGaP/GaAs heterojunction bipolar low-noise amplifier performance. Microelectronics Reliability, 2010, 50, 365-369.	0.9	0
141	Electrostatic Discharge (ESD) Protection Challenges of Gate-All-Around Nanowire Field-Effect Transistors. ECS Transactions, 2011, 34, 55-60.	0.3	0
142	Novel ESD protection solution for single-ended mixer in GaAs pHEMT technology. Microelectronics Reliability, 2013, 53, 952-955.	0.9	0
143	Study of graphene fieldâ€effect transistors under electrostatic discharge stresses. Electronics Letters, 2013, 49, 1086-1087.	0.5	0
144	Novel drain-less multi-gate pHEMT for electrostatic discharge (ESD) protection in GaAs technology. , 2013, , .		0

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145	Modern Phased Arrays and Their Hybrid Intelligent Processing. International Journal of Antennas and Propagation, 2014, 2014, 1-2.	0.7	0
146	Key factors affecting trigger voltage of SCRS for ESD protection. , 2014, , .		0
147	A reliability-boosted ferroelectric random access memory with random-dynamic reference cells. , 2014, , .		0
148	A new methodology for human metal model characterization. , 2015, , .		0
149	A novel vertical SCR for ESD protection in 40 V HV bipolar process. Microelectronics Reliability, 2017, 78, 307-310.	0.9	0
150	Editorial: IEDMS 2016. Microelectronics Reliability, 2018, 83, 207.	0.9	0
151	An Overview of On-Chip ESD Protection in Modern Deep Sub-Micron CMOS Technology. , 2018, , .		0
152	Statically triggered 3Ã—VDD-Tolerant ESD detection circuit in a 90-nm low-voltage CMOS process. Microelectronics Journal, 2018, 78, 88-93.	1.1	0
153	2Ã—VDD-tolerant ESD detection circuit in a 90-nm low-voltage CMOS process. , 2018, , .		0
154	Coupling Matrix Synthesis for the Cascaded Filters. , 2019, , .		0
155	A Robust Dual Directional SCR without Current Saturation Effect for ESD Applications. , 2019, , .		0
156	Investigation of the Filter Amplifiers using the TVS Diode for ESD Protection. , 2019, , .		0
157	Vertical bipolar junction transistor triggered siliconâ€controlled rectifier for nanoscale ESD engineering. Electronics Letters, 2020, 56, 350-351.	0.5	0
158	Electrical Conductivity and Thermal Sensing of CNTs/Polymer Nanocomposites. , 2021, , .		0
159	Dynamic Tunable Absorber Based on VO2 Pyramid Array Structure Working in Infrared Band. , 2021, , .		0
160	Low Frequency Noise of the Tunneling Contact Thin-Film Transistors. , 2021, , .		0
161	A Special Section on: Next-Generation Electronics and Optoelectronics. Journal of Nanoelectronics and Optoelectronics, 2019, 14, 660-662.	0.1	0
162	Diode and RC Co-Triggered 2 Ã— VDD-Tolerant Electrostatic Discharge Detection Circuit in Nanoscale Complementary Metal-Oxide-Semiconductor Technology. Journal of Nanoelectronics and Optoelectronics, 2019, 14, 734-739.	0.1	0

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163	Characteristics of Tunnel Field-effect Transistors under Power-on Electrostatic Discharge and Electrical Overstress Conditions. Sensors and Materials, 2020, 32, 1889.	0.3	0
164	Reliability Issues of Thin Film Transistors Subject to Electrostatic Discharge Stresses: An Overview (Adv. Electron. Mater. 2/2022). Advanced Electronic Materials, 2022, 8, .	2.6	0