Salvatore Pennisi

List of Publications by Year in Descending Order

168 papers	2,526 citations	27 h-index	42 g-index
210 ext. papers	3,196 ext. citations	2.4 avg, IF	5.09 L-index

#	Paper	IF	Citations
168	A Novel Approach to Decay: PANDORA, a New Experimental Setup for Future In-Plasma Measurements. *Universe*, **2022**, 8, 80	2.5	2
167	Two-Stage OTA with all Subthreshold MOSFETs and Optimum GBW to DC-Current Ratio. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2022**, 1-1	3.5	
166	A Biasing Approach to Design Ultra-Low-Power Standard-Cell-Based Analog Building Blocks for Nanometer SoCs. *IEEE Access*, **2022**, 10, 25892-25900	3.5	3
165	A 0.5 V Sub-Threshold CMOS Current-Controlled Ring Oscillator for IoT and Implantable Devices. *Journal of Low Power Electronics and Applications*, **2022**, 12, 16	1.7	1
164	0.5 V CMOS Inverter-Based Transconductance Amplifier with Quiescent Current Control. *Journal of Low Power Electronics and Applications*, **2021**, 11, 37	1.7	5
163	High-Frequency Low-Current Second-Order Bandpass Active Filter Topology and Its Design in 28-nm FD-SOI CMOS. *Journal of Low Power Electronics and Applications*, **2020**, 10, 27	1.7	3
162	Sub-Femto-Farad Resolution Electronic Interfaces for Integrated Capacitive Sensors: A Review. *IEEE Access*, **2020**, 8, 153969-153980	3.5	15
161	0.6-V CMOS cascode OTA with complementary gate-driven gain-boosting and forward body bias. *International Journal of Circuit Theory and Applications*, **2020**, 48, 15-27	2	12
160	Active load with cross-coupled bulk for high-gain high-CMRR nanometer CMOS differential stages. *International Journal of Circuit Theory and Applications*, **2019**, 47, 1700-1704	2	6
159	Class-AB CMOS output stages suitable for low-voltage amplifiers in nanometer technologies. *Microelectronics Journal*, **2019**, 92, 104597	1.8	4
158	Autonomous Energy-Efficient Wireless Sensor Network Platform for Home/Office Automation. *IEEE Sensors Journal*, **2019**, 19, 3501-3512	4	48
157	High-Performance Three-Stage Single-Miller CMOS OTA With No Upper Limit of ${C}_{L}$. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2018**, 65, 1529-1533	3.5	21
156	A rail-to-rail constant-gm CCII for Instrumentation Amplifier applications. *AEU - International Journal of Electronics and Communications*, **2018**, 91, 103-109	2.8	14
155	Dual PushPull High-Speed Rail-to-Rail CMOS Buffer Amplifier for Flat-Panel Displays. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2018**, 65, 1879-1883	3.5	8
154	Switched-Capacitor Power Management Integrated Circuit for Autonomous Internet of Things Node. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2018**, 65, 1455-1459	3.5	15
153	Ultra-Low Power Amplifiers for IoT Nodes **2018**,		5
152	0.9-V Class-AB Miller OTA in 0.35- $mu text{m}$ CMOS With Threshold-Lowered Non-Tailed Differential Pair. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2017**, 64, 1740-1747	3.9	31

151	The noise performance of CMOS Miller operational transconductance amplifiers with embedded current-buffer frequency compensation. *International Journal of Circuit Theory and Applications*, **2017**, 45, 457-465	2	4
150	Optimized Active Single-Miller Capacitor Compensation With Inner Half-Feedforward Stage for Very High-Load Three-Stage OTAs. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2016**, 63, 1349-1359	3.9	32
149	0.7-V Three-Stage Class-AB CMOS Operational Transconductance Amplifier. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2016**, 63, 1807-1815	3.9	66
148	Symbolic factorization methodology for multistage amplifier transfer functions. *International Journal of Circuit Theory and Applications*, **2016**, 44, 38-59	2	12
147	Improved single-miller passive compensation network for three-stage CMOS OTAs. *Analog Integrated Circuits and Signal Processing*, **2016**, 86, 417-427	1.2	11
146	CMOS Non-tailed differential pair. *International Journal of Circuit Theory and Applications*, **2016**, 44, 1468-1477		4
145	Design Methodology of Subthreshold Three-Stage CMOS OTAs Suitable for Ultra-Low-Power Low-Area and High Driving Capability. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2015**, 62, 1453-1462	3.9	47
144	High-Performance Four-Stage CMOS OTA Suitable for Large Capacitive Loads. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2015**, 62, 2476-2484	3.9	41
143	Performance evaluation of a multistring photovoltaic module with distributed DC-DC converters. *IET Renewable Power Generation*, **2015**, 9, 935-942	2.9	20
142	Dovetail Tip: A New Approach for Low-Threshold Vacuum Nanoelectronics. *IEEE Transactions on Electron Devices*, **2015**, 62, 4293-4300	2.9	5
141	High-tuning-range CMOS band-pass IF filter based on a low-Q cascaded biquad optimization technique. *International Journal of Circuit Theory and Applications*, **2015**, 43, 1615-1636	2	7
140	Self-Biased Dual-Path Push-Pull Output Buffer Amplifier for LCD Column Drivers. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2014**, 61, 663-670	3.9	18
139	Low-Power Class-AB CMOS Voltage Feedback Current Operational Amplifier With Tunable Gain and Bandwidth. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2014**, 61, 574-578	3.5	12
138	88-mu A 1-MHz Stray-Insensitive CMOS Current-Mode Interface IC for Differential Capacitive Sensors. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2014**, 61, 1905-1916	3.9	29
137	A new accurate analytical expression for the SiPM transient response to single photons **2014**,		1
136	High-performance frequency compensation topology for four-stage OTAs **2014**,		7
135	Adaptive frequency compensation for maximum and constant bandwidth feedback amplifiers. *International Journal of Circuit Theory and Applications*, **2013**, 41, 424-440	2	3
134	4-Phase Interleaved Boost Converter With IC Controller for Distributed Photovoltaic Systems. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2013**, 60, 3090-3102	3.9	19

133	Micro-scale inductorless maximum power point tracking DC–DC converter. *IET Power Electronics*, **2013**, 6, 1634-1639	2.2	14
132	Optimized frequency compensation topology for low-power three-stage OTAs **2013**,		1
131	Constant and maximum bandwidth feedback amplifier with adaptive frequency compensation **2012**,		3
130	Autotuning technique for CMOS current mode capacitive sensor interfaces **2012**,		1
129	Exploiting the Body of MOS Devices for High Performance Analog Design. *IEEE Circuits and Systems Magazine*, **2011**, 11, 8-23	3.2	29
128	**2011**,		7
127	Avoiding the Gain-Bandwidth Trade Off in Feedback Amplifiers. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2011**, 58, 2108-2113	3.9	15
126	Low-Power Cool Bypass Switch for Hot Spot Prevention in Photovoltaic Panels. *ETRI Journal*, **2011**, 33, 880-886	1.4	15
125	Self-biased dual-path push-pull output buffer amplifier topology for LCD driver applications **2011**,		1
124	**2011**,		1
123	Reply to "Comments on Avoiding the Gain-Bandwidth Trade Off in Feedback Amplifiers". *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2011**, 58, 2117-2117	3.9	1
122	IMPROVED LOW-POWER HIGH-SPEED BUFFER AMPLIFIER WITH SLEW-RATE ENHANCEMENT FOR LCD APPLICATIONS. *Journal of Circuits, Systems and Computers*, **2010**, 19, 325-334	0.9	7
121	Analytical figure of merit evaluation of RNMC networks for low-power three-stage OTAs **2010**,		1
120	A New Compact Low-Power High-Speed Rail-to-Rail Class-B Buffer for LCD Applications. *Journal of Display Technology*, **2010**, 6, 184-190		20
119	A 28mW WCDMA/GSM/GPRS/EDGE transformer-based receiver in 45nm CMOS **2010**,		1
118	Low-power high-speed rail-to-rail LCD output buffer with dual-path push–pull operation and quiescent current control. *Analog Integrated Circuits and Signal Processing*, **2010**, 65, 289-298	1.2	6
117	Step-response optimisation techniques for low-power, high-load, three-stage operational amplifiers driving large capacitive loads. *IET Circuits, Devices and Systems*, **2010**, 4, 87	1.1	10
116	Analytical comparison of reversed nested Miller frequency compensation techniques. *International Journal of Circuit Theory and Applications*, **2010**, 38, 709-737	2	42

115	A new advanced RNMC technique with dual-active current and voltage buffers for low-power high-load three-stage amplifiers **2009**,		2
114	IMPROVED POWER-EFFICIENT RNMC TECHNIQUE WITH VOLTAGE BUFFER AND NULLING RESISTORS FOR LOW-POWER HIGH-LOAD THREE-STAGE AMPLIFIERS. *Journal of Circuits, Systems and Computers*, **2009**, 18, 1321-1331	0.9	
113	670-nA CMOS OTA FOR AMLCD COLUMN DRIVER. *Journal of Circuits, Systems and Computers*, **2009**, 18, 339-350	0.9	4
112	Approach to analyse and design nearly sinusoidal oscillators. *IET Circuits, Devices and Systems*, **2009**, 3, 204-221	1.1	7
111	0.9-V CMOS cascode amplifier with body-driven gain boosting. *International Journal of Circuit Theory and Applications*, **2009**, 37, 193-202	2	25
110	Design Solutions for Sample-and-Hold Circuits in CMOS Nanometer Technologies. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2009**, 56, 459-463	3.5	24
109	Step-response optimization techniques for low-power three-stage operational amplifiers for large capacitive load applications **2009**,		2
108	An efficient RNM compensation topology with voltage buffer and nulling resistors for large-capacitive-load three-stage OTAs **2009**,		4
107	A high-speed low-power output buffer amplifier for large-size LCD applications **2009**,		2
106	Analysis and Implementation of a Minimum-Supply Body-Biased CMOS Differential Amplifier Cell. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2009**, 17, 172-180	2.6	18
105	Liquid Crystal Display Drivers **2009**,		47
104	Drivers for Active-Matrix LCDs **2009**, 189-235		
103	Unity-Gain Amplifier With Theoretically Zero Gain Error. *IEEE Transactions on Instrumentation and Measurement*, **2008**, 57, 1431-1437	5.2	4
102	Comparison of the Frequency Compensation Techniques for CMOS Two-Stage Miller OTAs. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2008**, 55, 1099-1103	3.5	24
101	A 2.5-GHz DDFS-PLL With 1.8-MHz Bandwidth in 0.35-mum CMOS. *IEEE Journal of Solid-State Circuits*, **2008**, 43, 1403-1413	5.5	16
100	Miller Theorem for Weakly Nonlinear Feedback Circuits and Application to CE Amplifier. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2008**, 55, 991-995	3.5	8
99	Wien-Type Oscillators: Evaluation and Optimization of Harmonic Distortion. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2008**, 55, 628-632	3.5	6
98	An approach to model high-frequency distortion in negative-feedback amplifiers. *International Journal of Circuit Theory and Applications*, **2008**, 36, 3-18	2	14

97	Analytical comparison of frequency compensation techniques in three-stage amplifiers. *International Journal of Circuit Theory and Applications*, **2008**, 36, 53-80	2	63
96	CMOS current-steering DAC architectures based on the triple-tail cell. *International Journal of Circuit Theory and Applications*, **2008**, 36, 233-246	2	5
95	Single Miller capacitor frequency compensation with nulling resistor for three-stage amplifiers. *International Journal of Circuit Theory and Applications*, **2008**, 36, 825-837	2	26
94	Design methodology of Miller frequency compensation with current buffer/amplifier. *IET Circuits, Devices and Systems*, **2008**, 2, 227	1.1	27
93	The Universal Circuit Simulator: A Mixed-Signal Approach to n-Port Network and Impedance Synthesis. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2007**, 54, 2178-2183	3.9	9
92	CMOS High-CMRR Current Output Stages. *IEEE Transactions on Circuits and Systems Part 2: Express Briefs*, **2007**, 54, 745-749		10
91	Distortion analysis in the frequency domain of a Gm-C biquad **2007**,		1
90	Two CMOS Current Feedback Operational Amplifiers. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2007**, 54, 944-948	3.5	17
89	Miller Compensation: Optimization with Current Buffer/Amplifier **2007**,		1
88	Design Procedures for Three-Stage CMOS OTAs With Nested-Miller Compensation. *IEEE Transactions on Circuits and Systems Part 1: Regular Papers*, **2007**, 54, 933-940		66
87	Linearization Technique for Source-Degenerated CMOS Differential Transconductors. *IEEE Transactions on Circuits and Systems Part 2: Express Briefs*, **2007**, 54, 848-852		28
86	CMOS Miller OTA with Body-Biased Output Stage **2007**,		2
85	Low quiescent current high speed amplifier for LCD column driver **2007**,		1
84	Very Low Voltage CMOS Two-stage Amplifier **2007**,		1
83	Advances in Reversed Nested Miller Compensation. *IEEE Transactions on Circuits and Systems Part 1: Regular Papers*, **2007**, 54, 1459-1470		113
82	Single Miller capacitor frequency compensation with nulling resistor for three-stage amplifiers **2007**,		4
81	Improved Reversed Nested Miller Frequency Compensation Technique With Voltage Buffer and Resistor. *IEEE Transactions on Circuits and Systems Part 2: Express Briefs*, **2007**, 54, 382-386		64
80	Sub-1V CMOS OTA with Body-driven Gain Boosting **2007**,		6

79	High-Drive and Linear CMOS Class-AB Pseudo-Differential Amplifier. *IEEE Transactions on Circuits and Systems Part 2: Express Briefs*, **2007**, 54, 112-116		6
78	Analog Path for Triple Band WCDMA Polar Modulated Transmitter in 90nm CMOS. *Radio Frequency Integrated Circuits (RFIC) Symposium, IEEE*, **2007**,		12
77	High-CMRR Current Amplifier Architecture and Its CMOS Implementation. *IEEE Transactions on Circuits and Systems Part 2: Express Briefs*, **2006**, 53, 1118-1122		11
76	Analysis of Harmonic Distortion in the Colpitts Oscillator **2006**,		2
75	Effects of nonlinear feedback in the frequency domain. *IEEE Transactions on Circuits and Systems Part 1: Regular Papers*, **2006**, 53, 225-234		22
74	Three-Stage CMOS OTA for Large Capacitive Loads With Efficient Frequency Compensation Scheme. *IEEE Transactions on Circuits and Systems Part 2: Express Briefs*, **2006**, 53, 1044-1048		60
73	High-speed CMOS unity-gain current amplifier. *Microelectronics Journal*, **2006**, 37, 1086-1091	1.8	8
72	Distortion analysis of Miller-compensated three-stage amplifiers. *IEEE Transactions on Circuits and Systems Part 1: Regular Papers*, **2006**, 53, 961-976		35
71	Nonidealities of Tow-Thomas biquads Using VOA- and CFOA-based Miller integrators. *IEEE Transactions on Circuits and Systems Part 2: Express Briefs*, **2005**, 52, 22-27		8
70	High-performance and simple CMOS interface circuit for differential capacitive sensors. *IEEE Transactions on Circuits and Systems Part 2: Express Briefs*, **2005**, 52, 327-330		21
69	Low-voltage high-drive CMOS current feedback op-amp. *IEEE Transactions on Circuits and Systems Part 2: Express Briefs*, **2005**, 52, 317-321		26
68	Accurate estimation of high-frequency harmonic distortion in two-stage Miller OTAs. *IET Circuits, Devices and Systems*, **2005**, 152, 417		20
67	Biasing technique via bulk terminal for minimum supply CMOS amplifiers. *Electronics Letters*, **2005**, 41, 779	1.1	20
66	Effect of CFOA nonidealities in Miller integrator cells. *IEEE Transactions on Circuits and Systems Part 2: Express Briefs*, **2004**, 51, 249-253		3
65	High-CMRR CMOS current output stage. *Electronics Letters*, **2003**, 39, 945	1.1	5
64	Design guidelines for reversed nested Miller compensation in three-stage amplifiers. *IEEE Transactions on Circuits and Systems Part 2: Express Briefs*, **2003**, 50, 227-233		84
63	Low-voltage CMOS current amplifier and its use for high-performance voltage amplification. *IET Circuits, Devices and Systems*, **2003**, 150, 205		10
62	CMOS single-input differential-output amplifier cells. *IET Circuits, Devices and Systems*, **2003**, 150, 194		4

61	1.5-V CMOS CCII+ with high current-driving capability. *IEEE Transactions on Circuits and Systems Part 2: Express Briefs*, **2003**, 50, 187-190		31
60	High-frequency harmonic distortion in feedback amplifiers: analysis and applications. *IEEE Transactions on Circuits and Systems Part 1: Regular Papers*, **2003**, 50, 328-340		49
59	Modelling of source-coupled logic gates. *International Journal of Circuit Theory and Applications*, **2002**, 30, 459-477	2	16
58	CMOS multiplier for grounded capacitors. *Electronics Letters*, **2002**, 38, 765	1.1	21
57	Pseudorandom bit generator based on dynamic linear feedback topology. *Electronics Letters*, **2002**, 38, 1097	1.1	11
56	Resolution of a current-mode algorithmic analog-to-digital converter. *IEEE Transactions on Circuits and Systems Part 1: Regular Papers*, **2002**, 49, 1480-1486		9
55	Current-mode A/D fuzzy converter. *IEEE Transactions on Fuzzy Systems*, **2002**, 10, 533-540	8.3	1
54	A low-voltage design approach for class AB current-mode circuits. *IEEE Transactions on Circuits and Systems Part 2: Express Briefs*, **2002**, 49, 273-279		22
53	Design methodology and advances in nested-Miller compensation. *IEEE Transactions on Circuits and Systems Part 1: Regular Papers*, **2002**, 49, 893-903		96
52	A high-performance CMOS CCII. *International Journal of Circuit Theory and Applications*, **2001**, 29, 331-336		8
51	Design Procedure for Two-Stage CMOS Transconductance Operational Amplifiers: A Tutorial. *Analog Integrated Circuits and Signal Processing*, **2001**, 27, 177-187	1.2	59
50	Current-feedback amplifiers versus voltage operational amplifiers. *IEEE Transactions on Circuits and Systems Part 1: Regular Papers*, **2001**, 48, 617-623		57
49	Analysis of the noise characteristics of current-feedback operational amplifier. *Microelectronics Reliability*, **2000**, 40, 321-327	1.2	1
48	Low-voltage dynamic biasing technique for CMOS class AB current-mode circuits. *Electronics Letters* , **2000**, 36, 114	1.1	7
47	Solutions for CMOS current amplifiers with high-drive output stages. *IEEE Transactions on Circuits and Systems Part 2: Express Briefs*, **2000**, 47, 988-998		12
46	Dynamic biasing for true low-voltage CMOS class AB current-mode circuits. *IEEE Transactions on Circuits and Systems Part 2: Express Briefs*, **2000**, 47, 1569-1575		27
45	High-performance and simple CMOS unity-gain amplifier. *IEEE Transactions on Circuits and Systems Part 1: Regular Papers*, **2000**, 47, 406-410		11
44	CMOS Current Amplifiers **1999**,		61

43	High-frequency CMOS amplifier with improved bandwidth performance. *Electronics Letters*, **1999**, 35, 1126	1.1	1
42	Design Strategies for Class A CMOS CCIIS. *Analog Integrated Circuits and Signal Processing*, **1999**, 19, 75-85	1.2	22
41	High-speed voltage buffers for the experimental characterization of CMOS transconductance operational amplifiers. *IEEE Transactions on Instrumentation and Measurement*, **1999**, 48, 31-33	5.2	0
40	Low-voltage class AB CMOS current output stage. *Electronics Letters*, **1999**, 35, 1329	1.1	11
39	High-Drive Current Amplifiers **1999**, 107-158		
38	Low-Drive Current Amplifiers **1999**, 45-106		1
37	Harmonic distortion in non-linear amplifier with non-linear feedback. *International Journal of Circuit Theory and Applications*, **1998**, 26, 293-299	2	3
36	High-drive CMOS current amplifier. *IEEE Journal of Solid-State Circuits*, **1998**, 33, 228-236	5.5	27
35	Harmonic distortion on class AB CMOS current output stages. *IEEE Transactions on Circuits and Systems Part 2: Express Briefs*, **1998**, 45, 243-250		24
34	High linearity CMOS current output stage. *Electronics Letters*, **1995**, 31, 789-790	1.1	27
33	A schmitt trigger by means of a ccii+. *International Journal of Circuit Theory and Applications*, **1995**, 23, 161-165	2	45
32	A novel CMOS current-mode power amplifier		4
31	Active capacitance multipliers using current conveyors		19
30	Analysis and evaluation of harmonic distortion in the tunnel diode oscillator		2
29	Distortion analysis of three-stage amplifiers with reversed nested-Miller compensation		2
28	High-performance CMOS pseudo-differential amplifier		11
27	Inverting closed-loop amplifier architecture with reduced gain error and high input impedance		1
26	Active reversed nested Miller compensation for three-stage amplifiers		15

25	Reversed Double Pole-Zero Cancellation Frequency Compensation Technique for Three-Stage Amplifiers	9
24	Current output stage with improved CMRR	2
23	Robust three-state PFD architecture with enhanced frequency acquisition capabilities	3
22	Harmonic distortion in three-stage nested-Miller-compensated amplifiers	5
21	High-performance CMOS current feedback operational amplifier	4
20	CMOS class AB single-to-differential transconductor	1
19	CMOS single-to-differential current amplifier	2
18	New analytical approach to evaluate harmonic distortion in nonlinear feedback amplifiers	1
17	Well-defined design procedure for a three-stage CMOS OTA	2
16	Feedback amplifiers: a simplified analysis of harmonic distortion in the frequency domain	2
15	Comparison between Miller integrator cells using VOAs and CFOAs	1
14	A novel pseudo random bit generator for cryptography applications	9
13	High accuracy CMOS capacitance multiplier	8
12	Reversed nested Miller compensation with voltage follower	3
11	Hybrid nested Miller compensation with nulling resistors	2
10	A new design approach for variable-gain low noise amplifiers	4
9	Reversed nested Miller compensation with current follower	5
8	High-drive CMOS current-feedback opamp	1

List of Publications

7	Filter circuits synthesis with CFOA-based differentiators		1
6	A versatile CMOS fully differential current amplifier		2
5	A low-voltage CMOS 1-Hz low-pass filter		9
4	A class AB CMOS current mirror with low-voltage capability		1
3	A CMOS operational floating conveyor		6
2	Single miller capacitor frequency compensation techniques: Theoretical comparison and critical review. *International Journal of Circuit Theory and Applications*,	2	1
1	Harmonic distortion in single-stage amplifiers		5