Salvatore Pennisi

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The third column is the impact factor (IF) of the journal, and the fourth column is the number of citations of the article.

168 papers	2,526 citations	27 h-index	42 g-index
210 ext. papers	3,196 ext. citations	2.4 avg, IF	5.09 L-index

#	Paper	IF	Citations
168	Advances in Reversed Nested Miller Compensation. *IEEE Transactions on Circuits and Systems Part 1: Regular Papers*, **2007**, 54, 1459-1470		113
167	Design methodology and advances in nested-Miller compensation. *IEEE Transactions on Circuits and Systems Part 1: Regular Papers*, **2002**, 49, 893-903		96
166	Design guidelines for reversed nested Miller compensation in three-stage amplifiers. *IEEE Transactions on Circuits and Systems Part 2: Express Briefs*, **2003**, 50, 227-233		84
165	0.7-V Three-Stage Class-AB CMOS Operational Transconductance Amplifier. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2016**, 63, 1807-1815	3.9	66
164	Design Procedures for Three-Stage CMOS OTAs With Nested-Miller Compensation. *IEEE Transactions on Circuits and Systems Part 1: Regular Papers*, **2007**, 54, 933-940		66
163	Improved Reversed Nested Miller Frequency Compensation Technique With Voltage Buffer and Resistor. *IEEE Transactions on Circuits and Systems Part 2: Express Briefs*, **2007**, 54, 382-386		64
162	Analytical comparison of frequency compensation techniques in three-stage amplifiers. *International Journal of Circuit Theory and Applications*, **2008**, 36, 53-80	2	63
161	CMOS Current Amplifiers **1999**,		61
160	Three-Stage CMOS OTA for Large Capacitive Loads With Efficient Frequency Compensation Scheme. *IEEE Transactions on Circuits and Systems Part 2: Express Briefs*, **2006**, 53, 1044-1048		60
159	Design Procedure for Two-Stage CMOS Transconductance Operational Amplifiers: A Tutorial. *Analog Integrated Circuits and Signal Processing*, **2001**, 27, 177-187	1.2	59
158	Current-feedback amplifiers versus voltage operational amplifiers. *IEEE Transactions on Circuits and Systems Part 1: Regular Papers*, **2001**, 48, 617-623		57
157	High-frequency harmonic distortion in feedback amplifiers: analysis and applications. *IEEE Transactions on Circuits and Systems Part 1: Regular Papers*, **2003**, 50, 328-340		49
156	Autonomous Energy-Efficient Wireless Sensor Network Platform for Home/Office Automation. *IEEE Sensors Journal*, **2019**, 19, 3501-3512	4	48
155	Design Methodology of Subthreshold Three-Stage CMOS OTAs Suitable for Ultra-Low-Power Low-Area and High Driving Capability. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2015**, 62, 1453-1462	3.9	47
154	Liquid Crystal Display Drivers **2009**,		47
153	A schmitt trigger by means of a ccii+. *International Journal of Circuit Theory and Applications*, **1995**, 23, 161-165	2	45
152	Analytical comparison of reversed nested Miller frequency compensation techniques. *International Journal of Circuit Theory and Applications*, **2010**, 38, 709-737	2	42

151	High-Performance Four-Stage CMOS OTA Suitable for Large Capacitive Loads. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2015**, 62, 2476-2484	3.9	41
150	Distortion analysis of Miller-compensated three-stage amplifiers. *IEEE Transactions on Circuits and Systems Part 1: Regular Papers*, **2006**, 53, 961-976		35
149	Optimized Active Single-Miller Capacitor Compensation With Inner Half-Feedforward Stage for Very High-Load Three-Stage OTAs. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2016**, 63, 1349-1359	3.9	32
148	0.9-V Class-AB Miller OTA in 0.35- $mu text{m}$ CMOS With Threshold-Lowered Non-Tailed Differential Pair. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2017**, 64, 1740-1747	3.9	31
147	1.5-V CMOS CCII+ with high current-driving capability. *IEEE Transactions on Circuits and Systems Part 2: Express Briefs*, **2003**, 50, 187-190		31
146	88-mu A 1-MHz Stray-Insensitive CMOS Current-Mode Interface IC for Differential Capacitive Sensors. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2014**, 61, 1905-1916	3.9	29
145	Exploiting the Body of MOS Devices for High Performance Analog Design. *IEEE Circuits and Systems Magazine*, **2011**, 11, 8-23	3.2	29
144	Linearization Technique for Source-Degenerated CMOS Differential Transconductors. *IEEE Transactions on Circuits and Systems Part 2: Express Briefs*, **2007**, 54, 848-852		28
143	Design methodology of Miller frequency compensation with current buffer/amplifier. *IET Circuits, Devices and Systems*, **2008**, 2, 227	1.1	27
142	Dynamic biasing for true low-voltage CMOS class AB current-mode circuits. *IEEE Transactions on Circuits and Systems Part 2: Express Briefs*, **2000**, 47, 1569-1575		27
141	High-drive CMOS current amplifier. *IEEE Journal of Solid-State Circuits*, **1998**, 33, 228-236	5.5	27
140	High linearity CMOS current output stage. *Electronics Letters*, **1995**, 31, 789-790	1.1	27
139	Single Miller capacitor frequency compensation with nulling resistor for three-stage amplifiers. *International Journal of Circuit Theory and Applications*, **2008**, 36, 825-837	2	26
138	Low-voltage high-drive CMOS current feedback op-amp. *IEEE Transactions on Circuits and Systems Part 2: Express Briefs*, **2005**, 52, 317-321		26
137	0.9-V CMOS cascode amplifier with body-driven gain boosting. *International Journal of Circuit Theory and Applications*, **2009**, 37, 193-202	2	25
136	Design Solutions for Sample-and-Hold Circuits in CMOS Nanometer Technologies. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2009**, 56, 459-463	3.5	24
135	Comparison of the Frequency Compensation Techniques for CMOS Two-Stage Miller OTAs. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2008**, 55, 1099-1103	3.5	24
134	Harmonic distortion on class AB CMOS current output stages. *IEEE Transactions on Circuits and Systems Part 2: Express Briefs*, **1998**, 45, 243-250		24

133	Effects of nonlinear feedback in the frequency domain. *IEEE Transactions on Circuits and Systems Part 1: Regular Papers*, **2006**, 53, 225-234		22
132	A low-voltage design approach for class AB current-mode circuits. *IEEE Transactions on Circuits and Systems Part 2: Express Briefs*, **2002**, 49, 273-279		22
131	Design Strategies for Class A CMOS CCIIS. *Analog Integrated Circuits and Signal Processing*, **1999**, 19, 75-85	1.2	22
130	High-Performance Three-Stage Single-Miller CMOS OTA With No Upper Limit of ${C}_{L}$. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2018**, 65, 1529-1533	3.5	21
129	High-performance and simple CMOS interface circuit for differential capacitive sensors. *IEEE Transactions on Circuits and Systems Part 2: Express Briefs*, **2005**, 52, 327-330		21
128	CMOS multiplier for grounded capacitors. *Electronics Letters*, **2002**, 38, 765	1.1	21
127	Performance evaluation of a multistring photovoltaic module with distributed DC-DC converters. *IET Renewable Power Generation*, **2015**, 9, 935-942	2.9	20
126	A New Compact Low-Power High-Speed Rail-to-Rail Class-B Buffer for LCD Applications. *Journal of Display Technology*, **2010**, 6, 184-190		20
125	Accurate estimation of high-frequency harmonic distortion in two-stage Miller OTAs. *IET Circuits, Devices and Systems*, **2005**, 152, 417		20
124	Biasing technique via bulk terminal for minimum supply CMOS amplifiers. *Electronics Letters*, **2005**, 41, 779	1.1	20
123	4-Phase Interleaved Boost Converter With IC Controller for Distributed Photovoltaic Systems. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2013**, 60, 3090-3102	3.9	19
122	Active capacitance multipliers using current conveyors		19
121	Self-Biased Dual-Path Push-Pull Output Buffer Amplifier for LCD Column Drivers. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2014**, 61, 663-670	3.9	18
120	Analysis and Implementation of a Minimum-Supply Body-Biased CMOS Differential Amplifier Cell. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2009**, 17, 172-180	2.6	18
119	Two CMOS Current Feedback Operational Amplifiers. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2007**, 54, 944-948	3.5	17
118	A 2.5-GHz DDFS-PLL With 1.8-MHz Bandwidth in 0.35-mum CMOS. *IEEE Journal of Solid-State Circuits*, **2008**, 43, 1403-1413	5.5	16
117	Modelling of source-coupled logic gates. *International Journal of Circuit Theory and Applications*, **2002**, 30, 459-477	2	16
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115	Avoiding the Gain-Bandwidth Trade Off in Feedback Amplifiers. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2011**, 58, 2108-2113	3.9	15
114	Low-Power Cool Bypass Switch for Hot Spot Prevention in Photovoltaic Panels. *ETRI Journal*, **2011**, 33, 880-886	1.4	15
113	Active reversed nested Miller compensation for three-stage amplifiers		15
112	Sub-Femto-Farad Resolution Electronic Interfaces for Integrated Capacitive Sensors: A Review. *IEEE Access*, **2020**, 8, 153969-153980	3.5	15
111	A rail-to-rail constant-gm CCII for Instrumentation Amplifier applications. *AEU - International Journal of Electronics and Communications*, **2018**, 91, 103-109	2.8	14
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93	Reversed Double Pole-Zero Cancellation Frequency Compensation Technique for Three-Stage Amplifiers		9
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91	Resolution of a current-mode algorithmic analog-to-digital converter. *IEEE Transactions on Circuits and Systems Part 1: Regular Papers*, **2002**, 49, 1480-1486		9
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71	Dovetail Tip: A New Approach for Low-Threshold Vacuum Nanoelectronics. *IEEE Transactions on Electron Devices*, **2015**, 62, 4293-4300	2.9	5
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68	Harmonic distortion in three-stage nested-Miller-compensated amplifiers		5
67	Reversed nested Miller compensation with current follower		5
66	Harmonic distortion in single-stage amplifiers		5
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64	0.5 V CMOS Inverter-Based Transconductance Amplifier with Quiescent Current Control. *Journal of Low Power Electronics and Applications*, **2021**, 11, 37	1.7	5
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60	An efficient RNM compensation topology with voltage buffer and nulling resistors for large-capacitive-load three-stage OTAs **2009**,		4
59	A novel CMOS current-mode power amplifier		4
58	Unity-Gain Amplifier With Theoretically Zero Gain Error. *IEEE Transactions on Instrumentation and Measurement*, **2008**, 57, 1431-1437	5.2	4
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56	CMOS single-input differential-output amplifier cells. *IET Circuits, Devices and Systems*, **2003**, 150, 194		4
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44	A new advanced RNMC technique with dual-active current and voltage buffers for low-power high-load three-stage amplifiers **2009**,		2

43	Step-response optimization techniques for low-power three-stage operational amplifiers for large capacitive load applications **2009**,		2
42	A high-speed low-power output buffer amplifier for large-size LCD applications **2009**,		2
41	Analysis and evaluation of harmonic distortion in the tunnel diode oscillator		2
40	CMOS Miller OTA with Body-Biased Output Stage **2007**,		2
39	Distortion analysis of three-stage amplifiers with reversed nested-Miller compensation		2
38	Analysis of Harmonic Distortion in the Colpitts Oscillator **2006**,		2
37	Current output stage with improved CMRR		2
36	CMOS single-to-differential current amplifier		2
35	Well-defined design procedure for a three-stage CMOS OTA		2
34	Feedback amplifiers: a simplified analysis of harmonic distortion in the frequency domain		2
33	Hybrid nested Miller compensation with nulling resistors		2
32	A versatile CMOS fully differential current amplifier		2
31	A Novel Approach to Decay: PANDORA, a New Experimental Setup for Future In-Plasma Measurements. *Universe*, **2022**, 8, 80	2.5	2
30	A new accurate analytical expression for the SiPM transient response to single photons **2014**,		1
29	Optimized frequency compensation topology for low-power three-stage OTAs **2013**,		1
28	Analytical figure of merit evaluation of RNMC networks for low-power three-stage OTAs **2010**,		1
27	A 28mW WCDMA/GSM/GPRS/EDGE transformer-based receiver in 45nm CMOS **2010**,		1
26	Self-biased dual-path push-pull output buffer amplifier topology for LCD driver applications **2011**,		1

25	**2011**,		1
24	Reply to "Comments on Avoiding the Gain-Bandwidth Trade Off in Feedback Amplifiers". *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2011**, 58, 2117-2117	3.9	1
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22	Distortion analysis in the frequency domain of a Gm-C biquad **2007**,		1
21	Miller Compensation: Optimization with Current Buffer/Amplifier **2007**,		1
20	Low quiescent current high speed amplifier for LCD column driver **2007**,		1
19	Very Low Voltage CMOS Two-stage Amplifier **2007**,		1
18	Inverting closed-loop amplifier architecture with reduced gain error and high input impedance		1
17	CMOS class AB single-to-differential transconductor		1
16	New analytical approach to evaluate harmonic distortion in nonlinear feedback amplifiers		1
15	Comparison between Miller integrator cells using VOAs and CFOAs		1
14	Current-mode A/D fuzzy converter. *IEEE Transactions on Fuzzy Systems*, **2002**, 10, 533-540	8.3	1
13	Analysis of the noise characteristics of current-feedback operational amplifier. *Microelectronics Reliability*, **2000**, 40, 321-327	1.2	1
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11	Filter circuits synthesis with CFOA-based differentiators		1
10	High-frequency CMOS amplifier with improved bandwidth performance. *Electronics Letters*, **1999**, 35, 1126	1.1	1
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8	Single miller capacitor frequency compensation techniques: Theoretical comparison and critical review. *International Journal of Circuit Theory and Applications*,	2	1

7	Low-Drive Current Amplifiers **1999**, 45-106		1
6	A 0.5 V Sub-Threshold CMOS Current-Controlled Ring Oscillator for IoT and Implantable Devices. *Journal of Low Power Electronics and Applications*, **2022**, 12, 16	1.7	1
5	High-speed voltage buffers for the experimental characterization of CMOS transconductance operational amplifiers. *IEEE Transactions on Instrumentation and Measurement*, **1999**, 48, 31-33	5.2	0
4	IMPROVED POWER-EFFICIENT RNMC TECHNIQUE WITH VOLTAGE BUFFER AND NULLING RESISTORS FOR LOW-POWER HIGH-LOAD THREE-STAGE AMPLIFIERS. *Journal of Circuits, Systems and Computers*, **2009**, 18, 1321-1331	0.9	
3	High-Drive Current Amplifiers **1999**, 107-158		
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1	Two-Stage OTA with all Subthreshold MOSFETs and Optimum GBW to DC-Current Ratio. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2022**, 1-1	3.5	