Salvatore Pennisi

List of Publications by Year
in descending order

209	3,638	172443	206102
papers	citations	29 h-index	48 g-index

210	210	210	1241
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Advances in Reversed Nested Miller Compensation. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2007, 54, 1459-1470.	0.1	153
2	Design methodology and advances in nested-Miller compensation. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2002, 49, 893-903.	0.1	126
3	Design guidelines for reversed nested miller compensation in three-stage amplifiers. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2003, 50, 227-233.	2.2	111
4	0.7-V Three-Stage Class-AB CMOS Operational Transconductance Amplifier. IEEE Transactions on Circuits and Systems I: Regular Papers, 2016, 63, 1807-1815.	5.4	105
5	Design Procedure for Two-Stage CMOS Transconductance Operational Amplifiers: A Tutorial. Analog Integrated Circuits and Signal Processing, 2001, 27, 177-187.	1.4	93
6	CMOS Current Amplifiers. , 1999, , .		92
7	Analytical comparison of frequency compensation techniques in three-stage amplifiers. International Journal of Circuit Theory and Applications, 2008, 36, 53-80.	2.0	88
8	Design Procedures for Three-Stage CMOS OTAs With Nested-Miller Compensation. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2007, 54, 933-940.	0.1	85
9	Improved Reversed Nested Miller Frequency Compensation Technique With Voltage Buffer and Resistor. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2007, 54, 382-386.	2.2	84
10	Autonomous Energy-Efficient Wireless Sensor Network Platform for Home/Office Automation. IEEE Sensors Journal, 2019, 19, 3501-3512.	4.7	74
11	Current-feedback amplifiers versus voltage operational amplifiers. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2001, 48, 617-623.	0.1	72
12	Design Methodology of Subthreshold Three-Stage CMOS OTAs Suitable for Ultra-Low-Power Low-Area and High Driving Capability. IEEE Transactions on Circuits and Systems I: Regular Papers, 2015, 62, 1453-1462.	5.4	72
13	High-frequency harmonic distortion in feedback amplifiers: analysis and applications. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2003, 50, 328-340.	0.1	68
14	Three-Stage CMOS OTA for Large Capacitive Loads With Efficient Frequency Compensation Scheme. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2006, 53, 1044-1048.	2.2	68
15	High-Performance Four-Stage CMOS OTA Suitable for Large Capacitive Loads. IEEE Transactions on Circuits and Systems I: Regular Papers, 2015, 62, 2476-2484.	5.4	68
16	Analytical comparison of reversed nested Miller frequency compensation techniques. International Journal of Circuit Theory and Applications, 2010, 38, 709-737.	2.0	65
17	Liquid Crystal Display Drivers. , 2009, , .		64
18	Optimized Active Single-Miller Capacitor Compensation With Inner Half-Feedforward Stage for Very High-Load Three-Stage OTAs. IEEE Transactions on Circuits and Systems I: Regular Papers, 2016, 63, 1349-1359.	5.4	54

#	Article	IF	Citations
19	A schmitt trigger by means of a ccii+. International Journal of Circuit Theory and Applications, 1995, 23, 161-165.	2.0	51
20	0.9-V Class-AB Miller OTA in 0.35- $mu ext{m}$ CMOS With Threshold-Lowered Non-Tailed Differential Pair. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 1740-1747.	5.4	48
21	Distortion analysis of Miller-compensated three-stage amplifiers. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2006, 53, 961-976.	0.1	41
22	1.5-V CMOS CCII+ with high current-driving capability. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2003, 50, 187-190.	2.2	40
23	High-drive CMOS current amplifier. IEEE Journal of Solid-State Circuits, 1998, 33, 228-236.	5.4	39
24	Harmonic distortion on class AB CMOS current output stages. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 1998, 45, 243-250.	2.2	39
25	88-<formula formulatype="inline"><tex Notation="TeX">mu</tex> </formula>A 1-MHz Stray-Insensitive CMOS Current-Mode Interface IC for<newline/> Differential Capacitive Sensors. IEEE Transactions on Circuits and Systems I: Regular Papers, 2014, 61, 1905-1916.	5.4	39
26	Linearization Technique for Source-Degenerated CMOS Differential Transconductors. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2007, 54, 848-852.	2.2	38
27	Dynamic biasing for true low-voltage CMOS class AB current-mode circuits. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2000, 47, 1569-1575.	2.2	37
28	High-Performance Three-Stage Single-Miller CMOS OTA With No Upper Limit of <inline-formula> <tex-math notation="LaTeX">${C}_{L}$ </tex-math> </inline-formula>. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 1529-1533.	3.0	36
29	Design methodology of Miller frequency compensation with current buffer/amplifier. IET Circuits, Devices and Systems, 2008, 2, 227.	1.4	35
30	Low-voltage high-drive CMOS current feedback op-amp. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2005, 52, 317-321.	2.2	33
31	Comparison of the Frequency Compensation Techniques for CMOS Two-Stage Miller OTAs. IEEE Transactions on Circuits and Systems II: Express Briefs, 2008, 55, 1099-1103.	3.0	33
32	Exploiting the Body of MOS Devices for High Performance Analog Design. IEEE Circuits and Systems Magazine, 2011, 11, 8-23.	2.3	33
33	Sub-Femto-Farad Resolution Electronic Interfaces for Integrated Capacitive Sensors: A Review. IEEE Access, 2020, 8, 153969-153980.	4.2	33
34	High linearity CMOS current output stage. Electronics Letters, 1995, 31, 789-790.	1.0	32
35	Single Miller capacitor frequency compensation with nulling resistor for threeâ€stage amplifiers. International Journal of Circuit Theory and Applications, 2008, 36, 825-837.	2.0	31
36	Effects of nonlinear feedback in the frequency domain. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2006, 53, 225-234.	0.1	30

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37	0.9â€V CMOS cascode amplifier with bodyâ€driven gain boosting. International Journal of Circuit Theory and Applications, 2009, 37, 193-202.	2.0	29
38	Active capacitance multipliers using current conveyors. , 0, , .		28
39	Design Solutions for Sample-and-Hold Circuits in CMOS Nanometer Technologies. IEEE Transactions on Circuits and Systems II: Express Briefs, 2009, 56, 459-463.	3.0	28
40	A low-voltage design approach for class AB current-mode circuits. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2002, 49, 273-279.	2.2	27
41	Biasing technique via bulk terminal for minimum supply CMOS amplifiers. Electronics Letters, 2005, 41, 779.	1.0	27
42	High-performance and simple CMOS interface circuit for differential capacitive sensors. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2005, 52, 327-330.	2.2	27
43	A New Compact Low-Power High-Speed Rail-to-Rail Class-B Buffer for LCD Applications. Journal of Display Technology, 2010, 6, 184-190.	1.2	27
44	Self-Biased Dual-Path Push-Pull Output Buffer Amplifier for LCD Column Drivers. IEEE Transactions on Circuits and Systems I: Regular Papers, 2014, 61, 663-670.	5.4	27
45	CMOS multiplier for grounded capacitors. Electronics Letters, 2002, 38, 765.	1.0	26
46	Analysis and Implementation of a Minimum-Supply Body-Biased CMOS Differential Amplifier Cell. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2009, 17, 172-180.	3.1	25
47	Performance evaluation of a multistring photovoltaic module with distributed DCâ€“DC converters. IET Renewable Power Generation, 2015, 9, 935-942.	3.1	25
48	Design Strategies for Class A CMOS CCIIS. Analog Integrated Circuits and Signal Processing, 1999, 19, 75-85.	1.4	24
49	Active reversed nested Miller compensation for three-stage amplifiers. , 0, , .		24
50	A rail-to-rail constant-g m CCII for Instrumentation Amplifier applications. AEU - International Journal of Electronics and Communications, 2018, 91, 103-109.	2.9	24
51	Dual Pushâ€“Pull High-Speed Rail-to-Rail CMOS Buffer Amplifier for Flat-Panel Displays. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 1879-1883.	3.0	24
52	Accurate estimation of high-frequency harmonic distortion in two-stage Miller OTAs. IET Circuits, Devices and Systems, 2005, 152, 417.	0.6	23
53	4-Phase Interleaved Boost Converter With IC Controller for Distributed Photovoltaic Systems. IEEE Transactions on Circuits and Systems I: Regular Papers, 2013, 60, 3090-3102.	5.4	23
54	Low-Power Cool Bypass Switch for Hot Spot Prevention in Photovoltaic Panels. ETRI Journal, 2011, 33, 880-886.	2.0	22

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55	0.6â€V CMOS cascode OTA with complementary gateâ€driven gainâ€boosting and forward body bias. International Journal of Circuit Theory and Applications, 2020, 48, 15-27.	2.0	22
56	A 2.5-GHz DDFS-PLL With 1.8-MHz Bandwidth in 0.35-mum CMOS. IEEE Journal of Solid-State Circuits, 2008, 43, 1403-1413.	5.4	21
57	Modelling of source-coupled logic gates. International Journal of Circuit Theory and Applications, 2002, 30, 459-477.	2.0	20
58	Two CMOS Current Feedback Operational Amplifiers. IEEE Transactions on Circuits and Systems II: Express Briefs, 2007, 54, 944-948.	3.0	20
59	An approach to model high-frequency distortion in negative-feedback amplifiers. International Journal of Circuit Theory and Applications, 2008, 36, 3-18.	2.0	20
60	Microâ€scale inductorless maximum power point tracking DCâ€“DC converter. IET Power Electronics, 2013, 6, 1634-1639.	2.1	20
61	Switched-Capacitor Power Management Integrated Circuit for Autonomous Internet of Things Node. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 1455-1459.	3.0	20
62	Solutions for CMOS current amplifiers with high-drive output stages. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2000, 47, 988-998.	2.2	19
63	A Novel Approach to Î²-Decay: PANDORA, a New Experimental Setup for Future In-Plasma Measurements. Universe, 2022, 8, 80.	2.5	19
64	A novel pseudo random bit generator for cryptography applications. , 0, , .		16
65	Resolution of a current-mode algorithmic analog-to-digital converter. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2002, 49, 1480-1486.	0.1	16
66	High-CMRR Current Amplifier Architecture and Its CMOS Implementation. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2006, 53, 1118-1122.	2.2	16
67	Reversed Double Pole-Zero Cancellation Frequency Compensation Technique for Three-Stage Amplifiers. , 0, , .		16
68	Analog Path for Triple Band WCDMA Polar Modulated Transmitter in 90nm CMOS. Radio Frequency Integrated Circuits (RFIC) Symposium, IEEE, 2007, , .	0.0	16
69	Miller Theorem for Weakly Nonlinear Feedback Circuits and Application to CE Amplifier. IEEE Transactions on Circuits and Systems II: Express Briefs, 2008, 55, 991-995.	3.0	16
70	Avoiding the Gain-Bandwidth Trade Off in Feedback Amplifiers. IEEE Transactions on Circuits and Systems I: Regular Papers, 2011, 58, 2108-2113.	5.4	16
71	Improved single-miller passive compensation network for three-stage CMOS OTAs. Analog Integrated Circuits and Signal Processing, 2016, 86, 417-427.	1.4	16
72	A CMOS operational floating conveyor. , 0, , .		15

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73	High-performance and simple CMOS unity-gain amplifier. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2000, 47, 406-410.	0.1	15
74	Low-Power Class-AB CMOS Voltage Feedback Current Operational Amplifier With Tunable Gain and Bandwidth. IEEE Transactions on Circuits and Systems II: Express Briefs, 2014, 61, 574-578.	3.0	15
75	Pseudorandom bit generator based on dynamic linear feedback topology. Electronics Letters, 2002, 38, 1097.	1.0	14
76	Symbolic factorization methodology for multistage amplifier transfer functions. International Journal of Circuit Theory and Applications, 2016, 44, 38-59.	2.0	14
77	Ultra-Low Power Amplifiers for IoT Nodes. , 2018, , .		14
78	A new design approach for variable-gain low noise amplifiers. , 0, , .		13
79	Low-voltage CMOS current amplifier and its use for high-performance voltage amplification. IET Circuits, Devices and Systems, 2003, 150, 205.	0.6	13
80	CMOS High-CMRR Current Output Stages. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2007, 54, 745-749.	2.2	13
81	Step-response optimisation techniques for low-power, high-load, three-stage operational amplifiers driving large capacitive loads. IET Circuits, Devices and Systems, 2010, 4, 87.	1.4	13
82	A low-voltage CMOS 1-Hz low-pass filter. , 0, , .		12
83	Low-voltage class AB CMOS current output stage. Electronics Letters, 1999, 35, 1329.	1.0	12
84	High-Performance CMOS Pseudo-Differential Amplifier. , 0, , .		12
85	High-Drive and Linear CMOS Class-AB Pseudo-Differential Amplifier. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2007, 54, 112-116.	2.2	12
86	Design strategy for biquad-based continuous-time low-pass filters. , 2011, , .		12
87	0.5 V CMOS Inverter-Based Transconductance Amplifier with Quiescent Current Control. Journal of Low Power Electronics and Applications, 2021, 11, 37.	2.0	12
88	Low-voltage dynamic biasing technique for CMOS class AB current-mode circuits. Electronics Letters, 2000, 36, 114.	1.0	11
89	A high-performance CMOS CCII. International Journal of Circuit Theory and Applications, 2001, 29, 331-336.	2.0	11
90	High-speed CMOS unity-gain current amplifier. Microelectronics Journal, 2006, 37, 1086-1091.	2.0	11

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91	Sub-1V CMOS OTA with Body-driven Gain Boosting. , 2007, , .		11
92	Active load with crossâ€coupled bulk for highâ€gain highâ€CMRR nanometer CMOS differential stages. International Journal of Circuit Theory and Applications, 2019, 47, 1700-1704.	2.0	11
93	A Biasing Approach to Design Ultra-Low-Power Standard-Cell-Based Analog Building Blocks for Nanometer SoCs. IEEE Access, 2022, 10, 25892-25900.	4.2	11
94	High accuracy CMOS capacitance multiplier. , 0, , .		10
95	Low-power high-speed rail-to-rail LCD output buffer with dual-path pushâ€“pull operation and quiescent current control. Analog Integrated Circuits and Signal Processing, 2010, 65, 289-298.	1.4	10
96	IMPROVED LOW-POWER HIGH-SPEED BUFFER AMPLIFIER WITH SLEW-RATE ENHANCEMENT FOR LCD APPLICATIONS. Journal of Circuits, Systems and Computers, 2010, 19, 325-334.	1.5	10
97	Highâ€tuningâ€range CMOS bandâ€pass IF filter based on a lowâ€Q cascaded biquad optimization technique. International Journal of Circuit Theory and Applications, 2015, 43, 1615-1636.	2.0	10
98	Nonidealities of Tow-Thomas biquads Using VOA- and CFOA-based Miller integrators. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2005, 52, 22-27.	2.2	9
99	The Universal Circuit Simulator: A Mixed-Signal Approach to n-Port Network and Impedance Synthesis. IEEE Transactions on Circuits and Systems I: Regular Papers, 2007, 54, 2178-2183.	5.4	9
100	Wien-Type Oscillators: Evaluation and Optimization of Harmonic Distortion. IEEE Transactions on Circuits and Systems II: Express Briefs, 2008, 55, 628-632.	3.0	9
101	High-performance frequency compensation topology for four-stage OTAs. , 2014, , .		9
102	Harmonic distortion in single-stage amplifiers. , 0, , .		8
103	New CMOS tunable transconductor for filtering applications. , 0, , .		8
104	High-CMRR CMOS current output stage. Electronics Letters, 2003, 39, 945.	1.0	8
105	670-nA CMOS OTA FOR AMLCD COLUMN DRIVER. Journal of Circuits, Systems and Computers, 2009, 18, 339-350.	1.5	8
106	Approach to analyse and design nearly sinusoidal oscillators. IET Circuits, Devices and Systems, 2009, 3, 204-221.	1.4	8
107	Dovetail Tip: A New Approach for Low-Threshold Vacuum Nanoelectronics. IEEE Transactions on Electron Devices, 2015, 62, 4293-4300.	3.0	8
108	High-Frequency Low-Current Second-Order Bandpass Active Filter Topology and Its Design in 28-nm FD-SOI CMOS. Journal of Low Power Electronics and Applications, 2020, 10, 27.	2.0	8

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109	The noise performance of CMOS Miller operational transconductance amplifiers with embedded currentâ€buffer frequency compensation. International Journal of Circuit Theory and Applications, 2017, 45, 457-465.	2.0	7
110	Class-AB CMOS output stages suitable for low-voltage amplifiers in nanometer technologies. Microelectronics Journal, 2019, 92, 104597.	2.0	7
111	Reversed nested Miller compensation with current follower. , 0, , .		6
112	Reversed nested Miller compensation with voltage follower. , 0, , .		6
113	Harmonic distortion in three-stage nested-Miller-compensated amplifiers. , 0, , .		6
114	Unity-Gain Amplifier With Theoretically Zero Gain Error. IEEE Transactions on Instrumentation and Measurement, 2008, 57, 1431-1437.	4.7	6
115	CMOS Nonâ€tailed differential pair. International Journal of Circuit Theory and Applications, 2016, 44, 1468-1477.	2.0	6
116	Single miller capacitor frequency compensation techniques: Theoretical comparison and critical review. International Journal of Circuit Theory and Applications, 2022, 50, 1462-1486.	2.0	6
117	A 0.5 V Sub-Threshold CMOS Current-Controlled Ring Oscillator for IoT and Implantable Devices. Journal of Low Power Electronics and Applications, 2022, 12, 16.	2.0	6
118	Harmonic distortion in non-linear amplifier with non-linear feedback. International Journal of Circuit Theory and Applications, 1998, 26, 293-299.	2.0	5
119	High-linear class AB transconductor for high-frequency applications. , 0, , .		5
120	High-performance CMOS Current Feedback Operational Amplifier. , 0, , .		5
121	Analysis and evaluation of harmonic distortion in the tunnel diode oscillator. , 0, , .		5
122	CMOS current-steering DAC architectures based on the triple-tail cell. International Journal of Circuit Theory and Applications, 2008, 36, 233-246.	2.0	5
123	A new advanced RNMC technique with dual-active current and voltage buffers for low-power high-load three-stage amplifiers. , 2009, , .		5
124	A new enhanced PSPICE implementation of the equivalent circuit model of SiPM detectors. , 2015, , .		5
125	Two-Stage OTA With All Subthreshold MOSFETs and Optimum GBW to DC-Current Ratio. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 3154-3158.	3.0	5
126	A novel CMOS current-mode power amplifier. , 0, , .		4

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127	A class AB CMOS current mirror with low-voltage capability. , 0, , .		4
128	CMOS single-input differential-output amplifier cells. IET Circuits, Devices and Systems, 2003, 150, 194.	0.6	4
129	Current output stage with improved CMRR. , 0, , .		4
130	Robust three-state PFD architecture with enhanced frequency acquisition capabilities. , 0, , .		4
131	Analysis of Harmonic Distortion in the Colpitts Oscillator. , 2006, , .		4
132	Single Miller capacitor frequency compensation with nulling resistor for three-stage amplifiers. , 2007, , .		4
133	Distortion analysis in the frequency domain of a G<inf>m</inf>-C biquad. , 2007, , .		4
134	Step-response optimization techniques for low-power three-stage operational amplifiers for large capacitive load applications. , 2009, , .		4
135	An efficient RNM compensation topology with voltage buffer and nulling resistors for large-capacitive-load three-stage OTAs. , 2009, , .		4
136	A low-quiescent current two-input/output buffer amplifier for LCDs. , 2012, , .		4
137	Filter circuits synthesis with CFOA-based differentiators. , 0, , .		3
138	A versatile CMOS fully differential current amplifier. , 0, , .		3
139	High-frequency CMOS amplifier with improved bandwidth performance. Electronics Letters, 1999, 35, 1126.	1.0	3
140	High-speed voltage buffers for the experimental characterization of CMOS transconductance operational amplifiers. IEEE Transactions on Instrumentation and Measurement, 1999, 48, 31-33.	4.7	3
141	Design guidelines for optimized nested Miller compensation. , 0, , .		3
142	Low-voltage continuous-time CMOS current amplifier with dynamic biasing. , 0, , .		3
143	Current-mode A/D fuzzy converter. IEEE Transactions on Fuzzy Systems, 2002, 10, 533-540.	9.8	3
144	Hybrid nested Miller compensation with nulling resistors. , 0, , .		3

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145	Effect of CFOA Nonidealities in Miller Integrator Cells. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2004, 51, 249-253.	2.2	3
146	New analytical approach to evaluate harmonic distortion in nonlinear feedback amplifiers. , 0, , .		3
147	CMOS Miller OTA with Body-Biased Output Stage. , 2007, , .		3
148	Very Low Voltage CMOS Two-stage Amplifier. , 2007, , .		3
149	A high-speed low-power output buffer amplifier for large-size LCD applications. , 2009, , .		3
150	Low-power dual-active class-AB buffer amplifier with self-biasing network for LCD column drivers. , 2010, , .		3
151	A 28mW WCDMA/GSM/GPRS/EDGE transformer-based receiver in 45nm CMOS. , 2010, , .		3
152	Self-biased dual-path push-pull output buffer amplifier topology for LCD driver applications. , 2011, , .		3
153	Constant and maximum bandwidth feedback amplifier with adaptive frequency compensation. , 2012, , .		3
154	Adaptive frequency compensation for maximum and constant bandwidth feedback amplifiers. International Journal of Circuit Theory and Applications, 2013, 41, 424-440.	2.0	3
155	Estimation of in-cylinder pressure using spark plug discharge current measurements. , 2013, , .		3
156	High-drive CMOS current-feedback opamp. , 0, , .		2
157	Analysis of the noise characteristics of current-feedback operational amplifier. Microelectronics Reliability, 2000, 40, 321-327.	1.7	2
158	Delay estimation of SCL gates with output buffer. , 0, , .		2
159	Feedback amplifiers: a simplified analysis of harmonic distortion in the frequency domain. , 0, , .		2
160	Comparison between Miller integrator cells using VOAs and CFOAs. , 0, , .		2
161	CMOS Single-to-Differential Current Amplifier. , 0, , .		2
162	Well-Defined Design Procedure for a Three-Stage CMOS OTA. , 0, , .		2

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163	Distortion analysis of three-stage amplifiers with reversed nested-Miller compensation. , 0, , .		2
164	Inverting closed-loop amplifier architecture with reduced gain error and high input impedance. , 0, , .		2
165	150 Î¼A CMOS Transconductor with 82 dB SFDR. , 2007, , .		2
166	Miller Compensation: Optimization with Current Buffer/Amplifier. , 2007, , .		2
167	Design guidelines for minimum harmonic distortion in a wien oscillator with automatic amplitude control system. , 2008, , .		2
168	Analytical figure of merit evaluation of RNMC networks for low-power three-stage OTAs. , 2010, , .		2
169	0.13-µm CMOS tunable transconductor based on the body-driven gain boosting technique with application in Gm-C filters. , 2011, , .		2
170	Autotuning technique for CMOS current mode capacitive sensor interfaces. , 2012, , .		2
171	Three-stage single-miller CMOS OTA driving 10 nF with 1.46-MHz GBW. , 2018, , .		2
172	Performance parameters of current operational amplifiers. , 0, , .		1
173	Low-voltage CMOS current operational amplifier with class AB input stage. , 0, , .		1
174	Statistical analysis of the resolution in a current-mode ADC. , 0, , .		1
175	CMOS class AB single-to-differential transconductor. , 0, , .		1
176	Switched-capacitor body-biasing technique for very low voltage CMOS amplifiers. , 0, , .		1
177	Current-steering D/A converter based on triple tail cell. , 0, , .		1
178	Low quiescent current high speed amplifier for LCD column driver. , 2007, , .		1
179	CMOS body-enhanced cascode current mirror. , 2009, , .		1
180	A novel low-power high-speed rail-to-rail class-B buffer amplifier for LCD output drivers. , 2010, , .		1

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181	Reply to "Comments on Avoiding the Gain-Bandwidth Trade Off in Feedback Amplifiers". IEEE Transactions on Circuits and Systems I: Regular Papers, 2011, 58, 2117-2117.	5.4	1
182	Low voltage-drop bypass switch for photovoltaic applications. , 2012, , .		1
183	Effect of components relative tolerance in the magnitude response of a G<inf>m</inf>-C biquad. , 2013, , .		1
184	Optimized frequency compensation topology for low-power three-stage OTAs. , 2013, , .		1
185	A new accurate analytical expression for the SiPM transient response to single photons. , 2014, , .		1
186	Single-miller all-passive compensation network for three-stage OTAs. , 2015, , .		1
187	0.7-V bulk-driven three-stage class-AB OTA. , 2015, , .		1
188	A 0.003-mm2 50-mW three-stage amplifier driving 10-nF with 2.7-MHz GBW. , 2016, , .		1
189	Towards a nanofabricated vacuum cold-emitting triode. , 2017, , .		1
190	CMOS Differential Stage with Improved DC Gain, CMRR and PSRR Performance. , 2019, , .		1
191	Low-Drive Current Amplifiers. , 1999, , 45-106.		1
192	Single-Branch Wide-Swing-Cascode Subthreshold GaN Monolithic Voltage Reference. Electronics (Switzerland), 2022, 11, 1840.	3.1	1
193	Low harmonic distortion class AB CMOS current output stage. , 0, , .		0
194	Using a low-voltage COA for high-performance voltage amplification. , 0, , .		0
195	A tree-like amplifier architecture for large gain-bandwidth product. , 0, , .		0
196	Bipolar differential cell with improved bandwidth performance. , 0, , .		0
197	A charge injection based CMOS charge-pump. , 0, , .		0
198	2-V CMOS current operational amplifier with high CMRR. , 0, , .		0

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199	CMOS interface for differential capacitive transducers. , 0, , .		0
200	Source-degenerated CMOS Transconductor with Auxiliary Linearization. , 2007, , .		0
201	A generalization of Miller formulae for nonlinear feedback networks. , 2007, , .		0
202	CMOS voltage feedback current amplifier. , 2007, , .		0
203	Mixed-Signal Flexible Architecture for the Synthesis of ?-port Networks. , 2008, , .		0
204	IMPROVED POWER-EFFICIENT RNMC TECHNIQUE WITH VOLTAGE BUFFER AND NULLING RESISTORS FOR LOW-POWER HIGH-LOAD THREE-STAGE AMPLIFIERS. Journal of Circuits, Systems and Computers, 2009, 18, 1321-1331.	1.5	0
205	Exploitation of the phasor approach for closed-form solution of the Van der Pol's oscillator and sinusoidal oscillators with high-order nonlinearity. , 2009, , .		0
206	195-nW 120-dB subthreshold CMOS OTA driving up to 200 pF and occupying only 4.4â€“10â^'3 mm2. , 2015, , .		0
207	Drivers for Active-Matrix LCDs. , 2009, , 189-235.		0
208	High-Drive Current Amplifiers. , 1999, , 107-158.		0
209	A 0.5-V 28-nm CMOS Inverter-Based Comparator with Threshold Voltage Control. , 2022, , .		0