Yi Wang

List of Publications by Year
in descending order

27	507	840776 11	794594 19
papers	citations	h-index	g-index

27	27	27	330
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	MNFTL. , 2011, , .		89
2	A Space Reuse Strategy for Flash Translation Layers in SLC NAND Flash Memory Storage Systems. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2012, 20, 1094-1107.	3.1	50
3	Durable Address Translation in PCM-based Flash Storage Systems. IEEE Transactions on Parallel and Distributed Systems, 2016, , 1-1.	5.6	37
4	On-Demand Block-Level Address Mapping in Large-Scale NAND Flash Storage Systems. IEEE Transactions on Computers, 2014, , 1-1.	3.4	34
5	Meta-Cure. , 2012, , .		31
6	A Reliability Enhanced Address Mapping Strategy for Three-Dimensional (3-D) NAND Flash Memory. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 2402-2410.	3.1	28
7	Memory-Aware Task Scheduling with Communication Overhead Minimization for Streaming Applications on Bus-Based Multiprocessor System-on-Chips. IEEE Transactions on Parallel and Distributed Systems, 2014, 25, 1797-1807.	5.6	23
8	Heating Dispersal for Self-Healing NAND Flash Memory. IEEE Transactions on Computers, 2016, , 1-1.	3.4	20
9	A Reliability-Aware Address Mapping Strategy for NAND Flash Memory Storage Systems. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2014, 33, 1623-1631.	2.7	19
10	Towards Memory-Efficient Allocation of CNNs on Processing-in-Memory Architecture. IEEE Transactions on Parallel and Distributed Systems, 2018, 29, 1428-1441.	5.6	19
11	Exploiting Parallelism for CNN Applications on 3D Stacked Processing-In-Memory Architecture. IEEE Transactions on Parallel and Distributed Systems, 2019, 30, 589-600.	5.6	16
12	A Block-Level Log-Block Management Scheme for MLC NAND Flash Memory Storage Systems. IEEE Transactions on Computers, 2017, 66, 1464-1477.	3.4	15
13	P-Alloc. Transactions on Embedded Computing Systems, 2017, 16, 1-19.	2.9	15
14	Towards efficient allocation of graph convolutional networks on hybrid computation-in-memory architecture. Science China Information Sciences, 2021, 64, 1.	4.3	12
15	vFlash: Virtualized Flash for Optimizing the I/O Performance in Mobile Devices. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 1203-1214.	2.7	11
16	Alleviating Hot Data Write Back Effect for Shingled Magnetic Recording Storage Systems. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 2243-2254.	2.7	11
17	Temperature-Aware Persistent Data Management for LSM-Tree on 3-D NAND Flash Memory. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 4611-4622.	2.7	11
18	A Temperature-Aware Reliability Enhancement Strategy for 3-D Charge-Trap Flash Memory. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 234-244.	2.7	10

#	Article	IF	Citations
19	PATCH: Process-Variation-Resilient Space Allocation for Open-Channel SSD with 3D Flash. , 2019, , .		9
20	Formalization of continuous Fourier transform in verifying applications for dependable cyber-physical systems. Journal of Systems Architecture, 2020, 106, 101707.	4.3	9
21	DCR: Deterministic Crash Recovery for NAND Flash Storage Systems. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 2201-2214.	2.7	8
22	A Thermal-Aware Physical Space Reallocation for Open-Channel SSD With 3-D Flash Memory. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 617-627.	2.7	7
23	PVSensing: A Process-Variation-Aware Space Allocation Strategy for 3D NAND Flash Memory. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 1302-1315.	2.7	7
24	Tiler: An Autonomous Region-Based Scheme for SMR Storage. IEEE Transactions on Computers, 2021, 70, 291-304.	3.4	5
25	Temperature-aware data allocation strategy for 3D charge-trap flash memory. , 2017, , .		4
26	Optimally Removing Synchronization Overhead for CNNs in Three-Dimensional Neuromorphic Architecture. IEEE Transactions on Industrial Electronics, 2018, 65, 8973-8981.	7.9	4
27	Exploiting Parallelism for Convolutional Connections in Processing-In-Memory Architecture. , 2017, , .		3