Diana Marculescu

List of Publications by Year
in descending order

205 papers	4,764 citations
236925 25 h-index	223800 46 g-index
209 all docs	209 docs citations
209 times ranked	2416 citing authors

#	Article	IF	Citations
1	DeepNVM++: Cross-Layer Modeling and Optimization Framework of Nonvolatile Memories for Deep Learning. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 3426-3437.	2.7	8
2	Joslim: Joint Widths and Weights Optimization for Slimmable Neural Networks. Lecture Notes in Computer Science, 2021, , 119-134.	1.3	5
3	Width transfer: on the (in)variance of width optimization. , 2021, , .		3
4	Renofeation: A Simple Transfer Learning Method for Improved Adversarial Robustness. , 2021, , .		6
5	When Climate Meets Machine Learning: Edge to Cloud ML Energy Efficiency. , 2021, , .		2
6	ViP: Virtual Pooling for Accelerating CNN-based Image Classification and Object Detection. , 2020, , .		7
7	Towards Efficient Model Compression via Learned Global Ranking. , 2020, , .		83
8	Editorial: Special Issue on Compact Deep Neural Networks With Industrial Applications. IEEE Journal on Selected Topics in Signal Processing, 2020, 14, 605-608.	10.8	0
9	DeepNVM: A Framework for Modeling and Analysis of Non-Volatile Memory Technologies for Deep Learning Applications. , 2020, , .		10
10	Single-Path Mobile AutoML: Efficient ConvNet Design and NAS Hyperparameter Optimization. IEEE Journal on Selected Topics in Signal Processing, 2020, 14, 609-622.	10.8	21
11	Single-Path NAS: Designing Hardware-Efficient ConvNets in Less Than 4 Hours. Lecture Notes in Computer Science, 2020, , 481-497.	1.3	55
12	The Quest for Energy-Aware Computing: Confessions of an Accidental Engineer. Women in Engineering and Science, 2020, , 215-231.	0.4	0
13	One Weight Bitwidth to Rule Them All. Lecture Notes in Computer Science, 2020, , 85-103.	1.3	9
14	Edge AI. , 2020, , .		7
15	FLightNNs. , 2019, , .		14
16	Regularizing Activation Distribution for Training Binarized Deep Networks. , 2019, , .		67
17	Learning-Based Application-Agnostic 3D NoC Design for Heterogeneous Manycore Systems. IEEE Transactions on Computers, 2019, 68, 852-866.	3.4	47
18	Tractable Learning and Inference for Large-Scale Probabilistic Boolean Networks. IEEE Transactions on Neural Networks and Learning Systems, 2019, 30, 2720-2734.	11.3	9

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19	Profit: <underline>Pr</underline>iority and P<underline>o</underline>wer/Per<underline>f</underline>ormance Opt<underline>i</underline>miza<underline>t</underline>ion for Many-Core Systems. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 2064-2075.	2.7	7
20	Quantized deep neural networks for energy efficient hardware-based inference. , 2018, , .		31
21	On-Chip Communication Network for Efficient Training of Deep Convolutional Networks on Heterogeneous Manycore Systems. IEEE Transactions on Computers, 2018, 67, 672-686.	3.4	64
22	Understanding the Impact of Label Granularity on CNN-Based Image Classification. , 2018, , .		9
23	Designing adaptive neural networks for energy-constrained image classification. , 2018, , .		40
24	â€œWhere Are You Really From?â€♦ Mitigating Unconscious Bias on Campus. , 2018, , .		2
25	Hybrid on-chip communication architectures for heterogeneous manycore systems. , 2018, , .		4
26	Lightening the Load with Highly Accurate Storage- and Energy-Efficient LightNNs. ACM Transactions on Reconfigurable Technology and Systems, 2018, 11, 1-24.	2.5	10
27	Hardware-aware machine learning. , 2018, , .		27
28	HyperPower: Power- and memory-constrained hyper-parameter optimization for neural networks. , 2018, , .		37
29	Machine Learning and Manycore Systems Design: A Serendipitous Symbiosis. Computer, 2018, 51, 66-77.	1.1	54
30	Heterogeneous Dark Silicon Chip Multi-Processors: Design and Run-Time Management. , 2017, , 95-122.		0
31	Temperature Effect Inversion-Aware Power-Performance Optimization for FinFET-Based Multicore Systems. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 1897-1910.	2.7	6
32	LightNN. , 2017, , .		23
33	Imitation Learning for Dynamic VFI Control in Large-Scale Manycore Systems. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 2458-2471.	3.1	44
34	Thread Progress Equalization: Dynamically Adaptive Power-Constrained Performance Optimization of Multi-Threaded Applications. IEEE Transactions on Computers, 2017, 66, 731-744.	3.4	5
35	3D NoC-Enabled Heterogeneous Manycore Architectures for Accelerating CNN Training. , 2017, , .		13
36	M3A: Model, MetaModel and Anomaly Detection for Inter-arrivals of Web Searches and Postings. , 2017, , .		1

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37	Leveraging Classification Models for River Forecasting. , 2017, , .		0
38	Enhancing precipitation models by capturing multivariate and multiscale climate dynamics. , 2017, , .		1
39	Exploring aging deceleration in FinFET-based multi-core systems. , 2016, , .		12
40	A two-level approximate model driven framework for characterizing Multi-Cell Upsets impacts on processors. Microelectronics Journal, 2016, 48, 7-17.	2.0	5
41	Can We Guarantee Performance Requirements under Workload and Process Variations?. , 2016, , .		12
42	Hybrid network-on-chip architectures for accelerating deep learning kernels on heterogeneous manycore platforms. , 2016, , .		28
43	Wireless NoC and Dynamic VFI Codesign: Energy Efficiency Without Performance Penalty. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 2488-2501.	3.1	34
44	Learning-Based Power/Performance Optimization for Many-Core Systems With Extended-Range Voltage/Frequency Scaling. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, 35, 1318-1331.	2.7	12
45	A Support Vector Regression (SVR)-Based Latency Model for Network-on-Chip (NoC) Architectures. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, 35, 471-484.	2.7	38
46	Wireless NoC for VFI-Enabled Multicore Chip Design: Performance Evaluation and Design Trade-Offs. IEEE Transactions on Computers, 2016, 65, 1323-1336.	3.4	33
47	TEI-Turbo: temperature effect inversion-aware turbo boost for finfet-based multi-core systems. , 2015, , .		16
48	Distributed Reinforcement Learning for Power Limited Many-Core System Performance Optimization. , 2015, , .		60
49	Procrustes<xref rid="fn1" ref-type="fn"> <sup>1</sup> </xref>: Power Constrained Performance Improvement Using Extended Maximize-Then-Swap Algorithm. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2015, 34, 1664-1676.	2.7	14
50	Statistical learning in chip (SLIC). , 2015, , .		1
51	The quest for energy aware computing. , 2015, , .		1
52	The (low) power of less wiring: Enabling energy efficiency in many-core platforms through wireless NoC. , 2015, , .		2
53	Exploiting component dependency for accurate and efficient soft error analysis via Probabilistic Graphical Models. Microelectronics Reliability, 2015, 55, 251-263.	1.7	9
54	Energy efficient MapReduce with VFI-enabled multicore platforms. , 2015, , .		9

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55	Understanding and Using Heterogeneity for High Performance, Energy Efficient Computing: Special Session Extended Abstract. , 2015, , .		0
56	Energy-efficient VFI-partitioned multicore design using wireless NoC architectures. , 2014, , .		11
57	Statistical Peak Temperature Prediction and Thermal Yield Improvement for 3D Chip Multiprocessors. ACM Transactions on Design Automation of Electronic Systems, 2014, 19, 1-23.	2.6	18
58	SLIC: Statistical learning in chip. , 2014, , .		2
59	Power-Planning-Aware Soft Error Hardening via Selective Voltage Assignment. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 136-145.	3.1	5
60	A comprehensive and accurate latency model for Network-on-Chip performance analysis. , 2014, , .		23
61	The EDA Challenges in the Dark Silicon Era. , 2014, , .		153
62	Beyond Poisson: Modeling Inter-Arrival Time of Requests in a Datacenter. Lecture Notes in Computer Science, 2014, , 198-209.	1.3	25
63	Dynamic behavior of cell signaling networks. , 2013, , .		8
64	Cherry-Picking: Exploiting Process Variations in Dark-Silicon Homogeneous Chip Multi-Processors. , 2013, , .		70
65	A Low-Cost, Systematic Methodology for Soft Error Robustness of Logic Circuits. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 367-379.	3.1	25
66	HaDeS. , 2013, , .		43
67	SVR-NoC: A Performance Analysis Tool for Network-on-Chips Using Learning-based Support Vector Regression Model. , 2013, , .		37
68	Dynamic thread mapping for high-performance, power-efficient heterogeneous many-core systems. , 2013, , .		39
69	“Scaling” the impact of EDA education Preliminary findings from the CCC workshop series on extreme scale design automation. , 2013, , .		4
70	Impact of manufacturing process variations on performance and thermal characteristics of 3D ICs: Emerging challenges and new solutions. , 2013, , .		3
71	Mitigating the Impact of Process Variation on the Performance of 3-D Integrated Circuits. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 1903-1914.	3.1	8
72	Learning the optimal operating point for many-core systems with extended range voltage/frequency scaling. , 2013, , .		27

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73	Editorial to special section on networks on chip. ACM Transactions on Design Automation of Electronic Systems, 2013, 18, 1-2.	2.6	1
74	Hardware-efficient stereo estimation using a residual-based approach. , 2013, , .		2
75	Fundamental Limits on Run-Time Power Management Algorithms for MPSoCs. , 2013, , 1-21.		0
76	Technology-driven limits on runtime power management algorithms for multiprocessor systems-on-chip. ACM Journal on Emerging Technologies in Computing Systems, 2012, 8, 1-17.	2.3	7
77	Efficient on-line module-level wake-up scheduling for high performance multi-module designs. , 2012, , .		1
78	Mitigating lifetime underestimation: A system-level approach considering temperature variations and correlations between failure mechanisms. , 2012, , .		1
79	On the Impact of Manufacturing Process Variations on the Lifetime of Sensor Networks. Transactions on Embedded Computing Systems, 2012, 11, 1-13.	2.9	0
80	A learning-based autoregressive model for fast transient thermal analysis of chip-multiprocessors. , 2012, , .		34
81	Power-aware performance increase via core/uncore reinforcement control for chip-multiprocessors. , 2012, , .		37
82	Statistical thermal modeling and optimization considering leakage power variations. , 2012, , .		2
83	System-Level Leakage Variability Mitigation for MPSoC Platforms Using Body-Bias Islands. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2012, 20, 2289-2301.	3.1	12
84	Exploiting Process Variability in Voltage/Frequency Control. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2012, 20, 1392-1404.	3.1	40
85	Guest Editorial Special Section on PAR-CAD: Parallel CAD Algorithms and CAD for Parallel Architectures/Systems. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2012, 31, 7-8.	2.7	4
86	Statistical thermal evaluation and mitigation techniques for 3D Chip-Multiprocessors in the presence of process variations. , 2011, , .		10
87	Special session 4A: New topics parametric yield and reliability of 3D integrated circuits: New challenges and solutions. , 2011, , .		0
88	Analysis and mitigation of NBTI-induced performance degradation for power-gated circuits. , 2011, , .		7
89	Regulatory network analysis acceleration with reconfigurable hardware. , 2011, 2011, 149-52.		11
90	PRICE: Power reduction by placement and clock-network co-synthesis for pulsed-latch designs. , 2011, , .		4

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91	Aging-aware timing analysis and optimization considering path sensitization. , 2011, , .		12
92	Emulation of biological networks in reconfigurable hardware. , 2011, , .		13
93	Formal modeling and reasoning for reliability analysis. , 2010, , .		9
94	Clock skew scheduling for soft-error-tolerant sequential circuits. , 2010, , .		0
95	Custom feedback control. , 2010, , .		26
96	Multiple Transient Faults in Combinational and Sequential Circuits: A Systematic Approach. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2010, 29, 1614-1627.	2.7	94
97	Process variation aware performance modeling and dynamic power management for multi-core systems. , 2010, , .		0
98	Technology-driven limits on DVFS controllability of multiple voltage-frequency island designs. , 2009, , .		27
99	Integrating dynamic voltage/frequency scaling and adaptive body biasing using test-time voltage selection. , 2009, , .		8
100	A systematic approach to modeling and analysis of transient faults in logic circuits. , 2009, , .		19
101	Variation-aware dynamic voltage/frequency scaling. , 2009, , .		69
102	Mitigating the Impact of Variability on Chip-Multiprocessor Power and Performance. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2009, 17, 1520-1533.	3.1	9
103	Joint logic restructuring and pin reordering against NBTI-induced performance degradation. , 2009, , .		1
104	Design and Management of Voltage-Frequency Island Partitioned Networks-on-Chip. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2009, 17, 330-341.	3.1	120
105	3D-GCP: An analytical model for the impact of process variations on the critical path delay distribution of 3D ICs. , 2009, , .		28
106	System-level process variability analysis and mitigation for 3D MPSoCs. , 2009, , .		14
107	Power Management of Voltage/Frequency Island-Based Systems Using Hardware-Based Methods. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2009, 17, 427-438.	3.1	36
108	Post-floorplanning power/ground ring synthesis for multiple-supply-voltage designs. , 2009, , .		9

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109	Modeling and Optimization for Soft-Error Reliability of Sequential Circuits. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 803-816.	2.7	56
110	Process-Driven Variability Analysis of Single and Multiple Voltage–Frequency Island Latency-Constrained Systems. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 893-905.	2.7	13
111	Power-aware soft error hardening via selective voltage scaling. , 2008, , .		7
112	Process variability-aware transient fault modeling and analysis. , 2008, , .		14
113	Soft error rate reduction using redundancy addition and removal. , 2008, , .		0
114	Variability-Aware Frequency Scaling in Multi-Clock Processors. Integrated Circuits and Systems, 2008, , 207-227.	0.2	2
115	Variation-adaptive feedback control for networks-on-chip with multiple clock domains. , 2008, , .		65
116	Characterizing chip-multiprocessor variability-tolerance. , 2008, , .		48
117	System-level throughput analysis for process variation aware multiple voltage-frequency island designs. ACM Transactions on Design Automation of Electronic Systems, 2008, 13, 1-25.	2.6	169
118	Design Variability: Challenges and Solutions at Microarchitecture-Architecture Level. , 2008, , .		1
119	Guest Editorial Special Section on Low-Power Electronics and Design. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2008, 16, 609-610.	3.1	1
120	Celebration of the SIGDA CADathalon Winners. , 2008, , .		0
121	System-level mitigation of WID leakage power variability using body-bias islands. , 2008, , .		6
122	Soft Error Rate Analysis for Sequential Circuits. , 2007, , .		30
123	Voltage-frequency island partitioning for GALS-based networks-on-chip. Proceedings - Design Automation Conference, 2007, , .	0.0	98
124	On the impact of manufacturing process variations on the lifetime of sensor networks. , 2007, , .		7
125	MARS-S: Modeling and Reduction of Soft Errors in Sequential Circuits. , 2007, , .		17
126	Challenges and Promising Results in NoC Prototyping Using FPGAs. IEEE Micro, 2007, 27, 86-95.	1.8	31

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127	Architectures for silicon nanoelectronics and beyond. Computer, 2007, 40, 25-33.	1.1	74
128	System-Level Process Variation Driven Throughput Analysis for Single and Multiple Voltage-Frequency Island Designs. , 2007, , .		11
129	An 0.9 x 1.2", Low Power, Energy-Harvesting System with Custom Multi-Channel Communication Interface. , 2007, , .		10
130	Analysis of dynamic voltage/frequency scaling in chip-multiprocessors. , 2007, , .		269
131	Voltage-Frequency Island Partitioning for GALS-based Networks-on-Chip. Proceedings - Design Automation Conference, 2007, , .	0.0	5
132	Sunflower : Full-System, Embedded Microarchitecture Evaluation. Lecture Notes in Computer Science, 2007, , 168-182.	1.3	8
133	Celebration of the SIGDA CADathalon Winners. , 2007, , .		0
134	System-Level Process-Driven Variability Analysis for Single and Multiple Voltage-Frequency Island Systems. IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, 2006, , .	0.0	2
135	MARS-C. , 2006, , .		101
136	Circuit Reliability Analysis Using Symbolic Techniques. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2006, 25, 2638-2649.	2.7	87
137	Hardware based frequency/voltage control of voltage frequency island systems. , 2006, , .		26
138	System-level process-driven variability analysis for single and multiple voltage-frequency island systems. IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, 2006, , .	0.0	16
139	Increased Scalability and Power Efficiency by Using Multiple Speed Pipelines. Computer Architecture News, 2005, 33, 310-321.	2.5	3
140	Dynamic Functional Unit Assignment for Low Power. Journal of Supercomputing, 2005, 31, 47-62.	3.6	2
141	Undergraduate embedded system education at Carnegie Mellon. Transactions on Embedded Computing Systems, 2005, 4, 500-528.	2.9	61
142	Variability and energy awareness. , 2005, , .		64
143	Speed and voltage selection for GALS systems based on voltage/frequency islands. , 2005, , .		42
144	System level power and performance modeling of GALS point-to-point communication interfaces. , 2005, , .		11

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145	Energy Awareness and Uncertainty in Microarchitecture-Level Design. IEEE Micro, 2005, 25, 64-76.	1.8	25
146	Execution cache-based microarchitecture for power-efficient superscalar processors. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2005, 13, 14-26.	3.1	11
147	Toward a multiple clock/voltage island design style for power-aware processors. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2005, 13, 591-603.	3.1	35
148	Variability and energy awareness: a microarchitecture-level perspective. , 2005, , .		10
149	Modeling Computational, Sensing, and Acuation Surfaces. , 2005, , 16-1-16-14.		0
150	Impact of technology scaling on energy aware execution cache-based microarchitectures. , 2004, , .		0
151	Application adaptive energy efficient clustered architectures. , 2004, , .		7
152	E-textiles: toward computational clothing. IEEE Pervasive Computing, 2003, 2, 89-95.	1.3	7
153	Electronic textiles: a platform for pervasive computing. Proceedings of the IEEE, 2003, 91, 1993-1994.	21.3	9
154	Electronic textiles: a platform for pervasive computing. Proceedings of the IEEE, 2003, 91, 1995-2018.	21.3	249
155	Modeling, analysis, and self-management of electronic textiles. IEEE Transactions on Computers, 2003, 52, 996-1010.	3.4	27
156	Guest editors' introduction: Power and complexity aware design. IEEE Micro, 2003, 23, 8-11.	1.8	14
157	Ready to ware. IEEE Spectrum, 2003, 40, 28-32.	0.7	29
158	Fault-tolerant techniques for Ambient Intelligent distributed systems. , 2003, , .		4
159	A mixed-clock issue queue design for globally asynchronous, locally synchronous processor cores. , 2003, , .		1
160	A critical analysis of application-adaptive multiple clock processors. , 2003, , .		7
161	Dynamic Functional Unit Assignment for Low Power. , 2003, , 485-497.		0
162	Application Re-Mapping for Fault-Tolerance in Ambient Intelligent Systems. , 2003, , 315-335.		0

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163	Efficient Power/Performance Analysis of Embedded and General Purpose Software Applications. , 2003, , 289-303.		0
164	A mixed-clock issue queue design for globally asynchronous, locally synchronous processor cores. , 2003, , .		1
165	A critical analysis of application-adaptive multiple clock processors. , 2003, , .		0
166	Power efficiency of voltage scaling in multiple clock, multiple voltage cores. IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, 2002, , .	0.0	53
167	Power and performance evaluation of globally asynchronous locally synchronous processors. Computer Architecture News, 2002, 30, 158-168.	2.5	77
168	System and Microarchitectural Level Power Modeling, Optimization, and Their Implications in Energy Aware Computing. , 2002, , 241-276.		0
169	Challenges and opportunities in electronic textiles modeling and optimization. Proceedings - Design Automation Conference, 2002, , .	0.0	15
170	Challenges and opportunities in electronic textiles modeling and optimization. , 2002, , .		19
171	Microarchitecture-level power management. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2002, 10, 230-239.	3.1	16
172	Challenges and opportunities in electronic textiles modeling and optimization. Proceedings - Design Automation Conference, 2002, , .	0.0	0
173	Power reduction through work reuse. , 2001, , .		13
174	Stochastic sequential machine synthesis with application to constrained sequence generation. ACM Transactions on Design Automation of Electronic Systems, 2000, 5, 658-681.	2.6	4
175	Profile-driven code execution for low power dissipation (poster session). , 2000, , .		13
176	Theoretical bounds for switching activity analysis in finite-state machines. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2000, 8, 335-339.	3.1	9
177	Non-stationary effects in trace-driven power analysis. , 1999, , .		0
178	Sequence compaction for power estimation: theory and practice. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 1999, 18, 973-993.	2.7	35
179	Probabilistic modeling of dependencies during switching activity analysis. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 1998, 17, 73-83.	2.7	80
180	Theoretical bounds for switching activity analysis in finite-state machines. , 1998, , .		9

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181	Sequence compaction for probabilistic analysis of finite-state machines. , 1997, , .		12
182	Hierarchical sequence compaction for power estimation. , 1997, , .		17
183	Composite sequence compaction for finite-state machines using block entropy and high-order Markov models. , 1997, , .		11
184	Information theoretic measures for power analysis [logic design]. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 1996, 15, 599-610.	2.7	102
185	Stochastic sequential machine synthesis targeting constrained sequence generation. , 1996, , .		17
186	Improving the efficiency of power simulators by input vector compaction. , 1996, , .		29
187	Efficient power estimation for highly correlated input streams. , 1995, , .		63
188	Information theoretic measures of energy consumption at register transfer level. , 1995, , .		58
189	Efficient Power Estimation for Highly Correlated Input Streams. Proceedings - Design Automation Conference, 1995, , .	0.0	13
190	Improving the efficiency of power simulators by input vector compaction. , 0, , .		10
191	Stochastic sequential machine synthesis targeting constrained sequence generation. , 0, , .		14
192	Hierarchical Sequence Compaction For Power Estimation. , 0, , .		7
193	Sequence Compaction For Probabilistic Analysis Of Finite-state Machines. , 0, , .		3
194	Adaptive models for input data compaction for power simulators. , 0, , .		23
195	Trace-driven steady-state probability estimation in FSMs with application to power estimation. , 0, , .		13
196	Information-theoretic bounds for switching activity analysis in finite-state machines under temporally correlated inputs. , 0, , .		1
197	Power efficiency of voltage scaling in multiple clock multiple voltage cores. , 0, , .		8
198	Does Q = MC/sup 2/? (On the relationship between Quality in electronic design and the Model of) Tj ETQq0 0 0 rgBT /Overlock 10 Tf 50		7

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199	Ambient intelligence visions and achievements: linking abstract ideas to real-world concepts. , 0, , .		27
200	Toward an integrated design methodology for fault-tolerant, multiple clock/voltage integrated systems. , 0, , .		2
201	Increased Scalability and Power Efficiency by Using Multiple Speed Pipelines. , 0, , .		2
202	Energy Bounds for Fault-Tolerant Nanoscale Designs. , 0, , .		3
203	Composite sequence compaction for finite-state machines using block entropy and high-order Markov models. , 0, , .		1
204	Theoretical bounds for switching activity analysis in finite-state machines. , 0, , .		0
205	Non-stationary effects in trace-driven power analysis. , 0, , .		0