Young-Jae An

List of Publications by Year in descending order

Source: https://exaly.com/author-pdf/5133957/publications.pdf

Version: 2024-02-01

111 papers	1,398 citations	361296 20 h-index	434063 31 g-index
111 all docs	111 docs citations	111 times ranked	805 citing authors

#	Article	IF	Citations
1	A Novel Sensing Circuit for Deep Submicron Spin Transfer Torque MRAM (STT-MRAM). IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2012, 20, 181-186.	2.1	82
2	Comparative Study of Various Latch-Type Sense Amplifiers. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 425-429.	2.1	72
3	Power-Gated 9T SRAM Cell for Low-Energy Operation. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 1183-1187.	2.1	70
4	One-Sided Schmitt-Trigger-Based 9T SRAM Cell for Near-Threshold Operation. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 1551-1561.	3.5	64
5	A Magnetic Tunnel Junction Based Zero Standby Leakage Current Retention Flip-Flop. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2012, 20, 2044-2053.	2.1	56
6	A 10T-4MTJ Nonvolatile Ternary CAM Cell for Reliable Search Operation and a Compact Area. IEEE Transactions on Circuits and Systems II: Express Briefs, 2017, 64, 700-704.	2.2	40
7	STT-MRAM Sensing: A Review. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 12-18.	2.2	40
8	Reference-Scheme Study and Novel Reference Scheme for Deep Submicrometer STT-RAM. IEEE Transactions on Circuits and Systems I: Regular Papers, 2014, 61, 3376-3385.	3.5	39
9	A DLL With Dual Edge Triggered Phase Detector for Fast Lock and Low Jitter Clock Generator. IEEE Transactions on Circuits and Systems I: Regular Papers, 2012, 59, 1860-1870.	3.5	34
10	Process-Variation-Calibrated Multiphase Delay Locked Loop With a Loop-Embedded Duty Cycle Corrector. IEEE Transactions on Circuits and Systems II: Express Briefs, 2014, 61, 1-5.	2.2	33
11	An Energy Efficient Time-Domain Temperature Sensor for Low-Power On-Chip Thermal Management. IEEE Sensors Journal, 2014, 14, 104-110.	2.4	32
12	Single-Ended 9T SRAM Cell for Near-Threshold Voltage Operation With Enhanced Read Performance in 22-nm FinFET Technology. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 2748-2752.	2.1	31
13	Sense-Amplifier-Based Flip-Flop With Transition Completion Detection for Low-Voltage Operation. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 609-620.	2.1	29
14	A Split-Path Sensing Circuit for Spin Torque Transfer MRAM. IEEE Transactions on Circuits and Systems II: Express Briefs, 2014, 61, 193-197.	2.2	27
15	Process Variation Tolerant All-Digital 90^{circ} Phase Shift DLL for DDR3 Interface. IEEE Transactions on Circuits and Systems I: Regular Papers, 2012, 59, 2186-2196.	3.5	26
16	Single Bit-Line 7T SRAM Cell for Near-Threshold Voltage Operation With Enhanced Performance and Energy in 14 nm FinFET Technology. IEEE Transactions on Circuits and Systems I: Regular Papers, 2016, 63, 1023-1032.	3.5	25
17	STT-MRAM Sensing Circuit With Self-Body Biasing in Deep Submicron Technologies. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 1630-1634.	2.1	24
18	A Double-Sensing-Margin Offset-Canceling Dual-Stage Sensing Circuit for Resistive Nonvolatile Memory. IEEE Transactions on Circuits and Systems II: Express Briefs, 2015, 62, 1109-1113.	2.2	22

#	Article	IF	Citations
19	Sensing margin trend with technology scaling in MRAM. International Journal of Circuit Theory and Applications, 2011, 39, 313-325.	1.3	21
20	High-performance low-power magnetic tunnel junction based non-volatile flip-flop. , 2014, , .		21
21	An MTJâ€based nonâ€volatile flipâ€flop for highâ€performance SoC. International Journal of Circuit Theory and Applications, 2014, 42, 394-406.	1.3	20
22	Read Disturbance Reduction Technique for Offset-Canceling Dual-Stage Sensing Circuits in Deep Submicrometer STT-RAM. IEEE Transactions on Circuits and Systems II: Express Briefs, 2016, 63, 578-582.	2.2	18
23	Self-Timed Pulsed Latch for Low-Voltage Operation With Reduced Hold Time. IEEE Journal of Solid-State Circuits, 2019, 54, 2304-2315.	3.5	18
24	An Energy-Efficient All-Digital Time-Domain-Based CMOS Temperature Sensor for SoC Thermal Management. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 1508-1517.	2.1	17
25	An Offset-Tolerant Dual-Reference-Voltage Sensing Scheme for Deep Submicrometer STT-RAM. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 1361-1370.	2.1	17
26	Full-Swing Local Bitline SRAM Architecture Based on the 22-nm FinFET Technology for Low-Voltage Operation. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 1342-1350.	2.1	17
27	0.293-mm² Fast Transient Response Hysteretic Quasi-<inline-formula> <tex-math notation="LaTeX">V^{2} </tex-math> </inline-formula> DCâ€“DC Converter With Area-Efficient Time-Domain-Based Controller in 0.35-<inline-formula> <tex-math notation="LaTeX">mu </tex-math> </inline-formula>m CMOS. IEEE Journal of Solid-State Circuits, 2018, 53, 1844-1855.	3.5	17
28	A Decoder for Short BCH Codes With High Decoding Efficiency and Low Power for Emerging Memories. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 387-397.	2.1	16
29	All-Digital ON-Chip Process Sensor Using Ratioed Inverter-Based Ring Oscillator. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, , 1-11.	2.1	15
30	Offset-Cancellation Sensing-Circuit-Based Nonvolatile Flip-Flop Operating in Near-Threshold Voltage Region. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 2963-2972.	3.5	15
31	Offset-Compensated Cross-Coupled PFET Bit-Line Conditioning and Selective Negative Bit-Line Write Assist for High-Density Low-Power SRAM. IEEE Transactions on Circuits and Systems I: Regular Papers, 2015, , 1-9.	3.5	14
32	Trip-Point Bit-Line Precharge Sensing Scheme for Single-Ended SRAM. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 1370-1374.	2.1	14
33	Data-Cell-Variation-Tolerant Dual-Mode Sensing Scheme for Deep Submicrometer STT-RAM. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 163-174.	3.5	14
34	CNN Acceleration With Hardware-Efficient Dataflow for Super-Resolution. IEEE Access, 2020, 8, 187754-187765.	2.6	14
35	Switching pMOS Sense Amplifier for High-Density Low-Voltage Single-Ended SRAM. IEEE Transactions on Circuits and Systems I: Regular Papers, 2015, 62, 1555-1563.	3.5	13
36	High Performance and Self-rectifying Hafnia-based Ferroelectric Tunnel Junction for Neuromorphic Computing and TCAM Applications. , 2021, , .		13

#	Article	IF	Citations
37	All-Digital Fast-Locking Delay-Locked Loop Using a Cyclic-Locking Loop for DRAM. IEEE Transactions on Circuits and Systems II: Express Briefs, 2015, 62, 1023-1027.	2.2	11
38	High-Speed, Low-Power, and Highly Reliable Frequency Multiplier for DLL-Based Clock Generator. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 1484-1492.	2.1	11
39	Differential Read/Write 7T SRAM With Bit-Interleaved Structure for Near-Threshold Operation. IEEE Access, 2021, 9, 64105-64115.	2.6	11
40	A DLL based clock generator for low-power mobile SoCs. IEEE Transactions on Consumer Electronics, 2010, 56, 1950-1956.	3.0	10
41	Environmental-Variation-Tolerant Magnetic Tunnel Junction-Based Physical Unclonable Function Cell With Auto Write-Back Technique. IEEE Transactions on Information Forensics and Security, 2021, 16, 2843-2853.	4.5	10
42	Read-Preferred SRAM Cell With Write-Assist Circuit Using Back-Gate ETSOI Transistors in 22-nm Technology. IEEE Transactions on Electron Devices, 2012, 59, 2575-2581.	1.6	9
43	Integration of dual channel timing formatter system for high speed memory test equipment. , 2012, , .		9
44	A low-power and small-area all-digital delay-locked loop with closed-loop duty-cycle correction. , 2012, , .		9
45	All-digital process-variation-calibrated timing generator for ATE with 1.95-ps resolution and a maximum 1.2-GHz test rate. , 2013, , .		9
46	Thermal and solar energy harvesting boost converter with time-multiplexing MPPT algorithm. IEICE Electronics Express, 2016, 13, 20160287-20160287.	0.3	9
47	All-Digital 90Â° Phase-Shift DLL With Dithering Jitter Suppression Scheme. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 1015-1024.	2.1	9
48	Transient Cell Supply Voltage Collapse Write Assist Using Charge Redistribution. IEEE Transactions on Circuits and Systems II: Express Briefs, 2016, 63, 964-968.	2.2	9
49	All-Digital Process-Variation-Calibrated Timing Generator for ATE With 1.95-ps Resolution and Maximum 1.2-GHz Test Rate. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 1015-1025.	2.1	9
50	Sensing Margin Enhancement Technique Utilizing Boosted Reference Voltage for Low-Voltage and High-Density DRAM. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 2413-2422.	2.1	9
51	A Wide-Range Static Current-Free Current Mirror-Based LS With Logic Error Detection for Near-Threshold Operation. IEEE Journal of Solid-State Circuits, 2021, 56, 554-565.	3.5	9
52	MTJ based non-volatile flip-flop in deep submicron technology. , 2011, , .		8
53	Multiple-Cell Reference Scheme for Narrow Reference Resistance Distribution in Deep Submicrometer STT-RAM. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 2993-2997.	2.1	8
54	An Embedded Level-Shifting Dual-Rail SRAM for High-Speed and Low-Power Cache. IEEE Access, 2020, 8, 187126-187139.	2.6	8

#	Article	IF	Citations
55	Area- and Energy-Efficient STDP Learning Algorithm for Spiking Neural Network SoC. IEEE Access, 2020, 8, 216922-216932.	2.6	8
56	A comparative study of STT-MTJ based non-volatile flip-flops. , 2013, , .		7
57	Design of a 22-nm FinFET-Based SRAM With Read Buffer for Near-Threshold Voltage Operation. IEEE Transactions on Electron Devices, 2015, 62, 1698-1704.	1.6	7
58	Temperature-Tracking Sensing Scheme With Adaptive Precharge and Noise Compensation Scheme in PRAM. IEEE Transactions on Circuits and Systems I: Regular Papers, 2015, 62, 2091-2102.	3.5	7
59	Bitline Precharging and Preamplifying Switching pMOS for High-Speed Low-Power SRAM. IEEE Transactions on Circuits and Systems II: Express Briefs, 2016, 63, 1059-1063.	2.2	7
60	Pre-Charged Local Bit-Line Sharing SRAM Architecture for Near-Threshold Operation. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 2737-2747.	3.5	7
61	Non-Volatile Majority Function Logic Using Ferroelectric Memory for Logic in Memory Technology. IEEE Electron Device Letters, 2022, 43, 1049-1052.	2.2	7
62	Level-Converting Retention Flip-Flop for Reducing Standby Power in ZigBee SoCs. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 413-421.	2.1	6
63	Incremental Bitline Voltage Sensing Scheme With Half-Adaptive Threshold Reference Scheme in MLC PRAM. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 1444-1455.	3.5	6
64	GROâ€TDC with gateâ€switchâ€based delay cell halving resolution limit. International Journal of Circuit Theory and Applications, 2017, 45, 2211-2225.	1.3	6
65	Evaluation of STT-MRAM L3 cache in 7nm FinFET process. , 2018, , .		6
66	pMOS Pass Gate Local Bitline SRAM Architecture With Virtual $V_{mathrm{SS}}$ for Near-Threshold Operation. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 1079-1083.	2.1	6
67	A 6.9-Î¼m² 3.26-ns 31.25-fj Robust Level Shifter With Wide Voltage and Frequency Ranges. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 1433-1437.	2.2	6
68	Sensing circuit optimization using different type of transistors for deep submicron STT-RAM. , 2013, , .		5
69	Reference-circuit analysis for high-bandwidth spin transfer torque random access memory. , 2015, , .		5
70	Corner-Aware Dynamic Gate Voltage Scheme to Achieve High Read Yield in STT-RAM. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 2851-2860.	2.1	5
71	Variation-Tolerant WL Driving Scheme for High-Capacity NAND Flash Memory. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 1828-1839.	2.1	5
72	Adaptive Sensing Voltage Modulation Technique in Cross-Point OTS-PRAM. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021, 29, 631-642.	2.1	5

#	Article	IF	Citations
73	All-Bit-Line Read Scheme With Locking Bit-Line and Amplifying Sense Node in NAND Flash. IEEE Access, 2021, 9, 28001-28011.	2.6	5
74	SRAM Write- and Performance-Assist Cells for Reducing Interconnect Resistance Effects Increased With Technology Scaling. IEEE Journal of Solid-State Circuits, 2022, 57, 1039-1048.	3.5	5
75	ADDLL for Clock-Deskew Buffer in High-Performance SoCs. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 1368-1373.	2.1	4
76	One-Sided Static Noise Margin and Gaussian-Tail-Fitting Method for SRAM. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 1262-1269.	2.1	4
77	Comparative analysis of MCU memory for IoT application. , 2018, , .		4
78	Comparative Analysis of Digital STDP Learning Circuits Designed Using Counter and Shift Register. , 2019, , .		4
79	A Novel Matchline Scheduling Method for Low-Power and Reliable Search Operation in Cross-Point-Array Nonvolatile Ternary CAM. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 2650-2657.	2.1	4
80	A 90Â° phase-shift DLL with closed-loop DCC for high-speed mobile DRAM interface. IEEE Transactions on Consumer Electronics, 2010, 56, 2400-2405.	3.0	3
81	SRAM bitcell design for low voltage operation in deep submicron technologies. , 2011, , .		3
82	Dynamic mixed serialâ€“parallel content addressable memory (DMSP CAM). International Journal of Circuit Theory and Applications, 2013, 41, 721-731.	1.3	3
83	SRAM Design for 22-nm ETSOI Technology: Selective Cell Current Boosting and Asymmetric Back-Gate Write-Assist Circuit. IEEE Transactions on Circuits and Systems I: Regular Papers, 2015, 62, 1538-1545.	3.5	3
84	Area-optimal sensing circuit designs in deep submicrometer STT-RAM. , 2016, , .		3
85	Sensing voltage compensation circuit for low-power dram bit-line sense amplifier. , 2018, , .		3
86	A 0.166 pJ/b/pF, 3.5â€“5 Gb/s TSV I/O Interface With V_{OH} Drift Control. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 1822-1826.	2.2	3
87	A Sneak Current Compensation Scheme With Offset Cancellation Sensing Circuit for ReRAM-Based Cross-Point Memory Array. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 1583-1594.	3.5	3
88	Statistical modeling of layout-dependent characteristic fluctuations for multi-finger MOSFETs. , 2008, , .		2
89	Effects of Electrical Characteristics on the Non-Rectangular Gate Structure Variations for the Multifinger MOSFETs. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2011, 1, 352-358.	1.4	2
90	Static read stability and write ability metrics in FinFET based SRAM considering read and write-assist circuits. , 2012, , .		2

#	ARTICLE	IF	CITATIONS
91	All-digital 90° phase-shift DLL with a dithering jitter suppression scheme. , 2013, , .		2
92	Comparative analysis of 1:1:2 and 1:2:2 FinFET SRAM bit-cell using assist circuit. , 2013, , .		2
93	Pseudo NMOS based sense amplifier for high speed single-ended SRAM. , 2014, , .		2
94	Fast Monte-Carlo analysis method of ring oscillators with neural networks. , 2018, , .		2
95	Triplet-based Spike Timing Dependent Plasticity Circuit Design for three-terminal Spintronic Synapse. , 2018, , .		2
96	A 5 Gb/s Time-Interleaved Voltage-Mode Duobinary Encoding Scheme for 3-D-Stacked IC. IEEE Journal of Solid-State Circuits, 2022, 57, 1913-1923.	3.5	2
97	Impact of fin thickness and height on read stability / write ability in tri-gate FinFET based SRAM. , 2012, , .		1
98	Source follower based single ended sense amplifier for large capacity SRAM. , 2013, , .		1
99	Comparative analysis of using planar MOSFET and FinFET as access transistor of STT-RAM Cell in 22-nm technology node. , 2014, , .		1
100	Efficiency analysis of importance sampling in deep submicron STT-RAM design using uncontrollable industry-compatible model parameter. , 2015, , .		1
101	Low search power and high reliability 13T-4R MTJ based nonvolatile ternary content-addressable memory. , 2018, , .		1
102	Analysis on Sensing Yield of Voltage Latched Sense Amplifier for Low Power DRAM. , 2018, , .		1
103	SRAM Write Assist Circuit Using Cell Supply Voltage Self-Collapse With Bitline Charge Sharing for Near-Threshold Operation. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 1567-1571.	2.2	1
104	Imbalance-Tolerant Bit-Line Sense Amplifier for Dummy-Less Open Bit-Line Scheme in DRAM. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 2546-2554.	3.5	1
105	Equalization scheme analysis for high-density spin transfer torque random access memory. , 2016, , .		0
106	Low power SRAM bitcell design for near-threshold operation. , 2016, , .		0
107	Pulsed PMOS sense amplifier for high speed single-ended SRAM. , 2018, , .		0
108	Stepwise controlled voltage sensing scheme for high-density ReRAM with multi level cell. , 2018, , .		0

#	Article	IF	Citations
109	A Novel Heat-Aware Write Method with Optimized Heater Material and Structure in sub-20 nm PRAM for Low Energy Operation. , 2018, , .		0
110	Reliable Latency Extraction with NVSim Revision in Emerging NVM (ITC-CSCC 2019). , 2019, , .		0
111	High Performance and Area Efficient Ferroelectric FET based Reconfigurable Logic Circuit. , 2021, , .		0