Nikolaos Makris

List of Publications by Year
in descending order

23	167	1307594 7	1281871 11
papers	citations	h-index	g-index

23	23	23	137
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Comparison of Impact Ionization Models for 4H-SiC Along the <0001> Direction, Through Breakdown Voltage Simulations at Room Temperature. IEEE Transactions on Electron Devices, 2021, 68, 2582-2586.	3.0	2
2	Generalized Constant Current Method for Determining MOSFET Threshold Voltage. IEEE Transactions on Electron Devices, 2020, 67, 4559-4562.	3.0	12
3	Free Carrier Mobility, Series Resistance, and Threshold Voltage Extraction in Junction FETs. IEEE Transactions on Electron Devices, 2020, 67, 4658-4661.	3.0	2
4	Design of Micropower Operational Transconductance Amplifiers for High Total Ionizing Dose Effects. , 2019, , .		2
5	Compact Modeling of SiC and GaN Junction FETs at High Temperature. Materials Science Forum, 2019, 963, 683-687.	0.3	2
6	CJM: A Compact Model for Double-Gate Junction FETs. IEEE Journal of the Electron Devices Society, 2019, 7, 1191-1199.	2.1	8
7	FOSS EKV2.6 Verilog-A Compact MOSFET Model. , 2019, , .		4
8	Compact Modeling of Low Frequency Noise and Thermal Noise in Junction Field Effect Transistors. , 2019, , .		3
9	Forward and Reverse Operation of Enclosed-Gate MOSFETs and Sensitivity to High Total Ionizing Dose. , 2019, , .		0
10	Modeling of High Total Ionizing Dose (TID) Effects for Enclosed Layout Transistors in 65 nm Bulk CMOS. , 2018, , .		8
11	Investigation of Scaling and Temperature Effects in Total Ionizing Dose (TID) Experiments in 65 nm CMOS. , 2018, , .		5
12	A Compact Model for Static and Dynamic Operation of Symmetric Double-Gate Junction FETs. , 2018, , .		7
13	Charge-based Model for Junction FETs. IEEE Transactions on Electron Devices, 2018, 65, 2694-2698.	3.0	17
14	Total ionizing dose effects on analog performance of 65 nm bulk CMOS with enclosed-gate and standard layout. , 2018, , .		13
15	Charge-Based Modeling of Long-Channel Symmetric Double-Gate Junction FETsâ€”Part I: Drain Current and Transconductances. IEEE Transactions on Electron Devices, 2018, 65, 2744-2750.	3.0	9
16	Charge-Based Modeling of Long-Channel Symmetric Double-Gate Junction FETsâ€”Part II: Total Charges and Transcapacitances. IEEE Transactions on Electron Devices, 2018, 65, 2751-2756.	3.0	12
17	Variability of Low Frequency Noise and mismatch in enclosed-gate and standard nMOSFETs. , 2017, , .		5
18	Modelling of 4H-SiC VJFETs with Self-Aligned Contacts. Materials Science Forum, 2016, 858, 913-916.	0.3	3

#	Article	IF	Citations
19	Charge-Based Compact Model for Bias-Dependent Variability of 1/ f Noise in MOSFETs. IEEE Transactions on Electron Devices, 2016, 63, 4201-4208.	3.0	10
20	Openâ€source circuit simulation tools for RF compact semiconductor device modelling. International Journal of Numerical Modelling: Electronic Networks, Devices and Fields, 2014, 27, 761-779.	1.9	4
21	Modeling of highâ€frequency noise of silicon CMOS transistors for RFIC design. International Journal of Numerical Modelling: Electronic Networks, Devices and Fields, 2014, 27, 802-811.	1.9	1
22	CMOS Small-Signal and Thermal Noise Modeling at High Frequencies. IEEE Transactions on Electron Devices, 2013, 60, 3726-3733.	3.0	29
23	CMOS RF noise, scaling, and compact modeling for RFIC design. , 2013, , .		9