# David Z Pan

## List of Publications by Year in Descending Order



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|---|---|---|---|
| 153 papers | 1,911 citations | 23 h-index | 36 g-index |
| 176 ext. papers | 2,818 ext. citations | 3.4 avg, IF | 5.34 L-index |

| # | Paper | IF | Citations |
|---|---|---|---|
| 153 | A Broadband Spectrum Channelizer With PWM-LO-Based Sub-Band Gain Control. *IEEE Journal of Solid-State Circuits*, **2022**, 1-1 | 5.5 | 0 |
| 152 | Identification of 90 NAFLD GWAS loci and establishment of NAFLD PRS and causal role of NAFLD in coronary artery disease.. *Human Genetics and Genomics Advances*, **2022**, 3, 100056 | 0.8 | 0 |
| 151 | Tutorial and Perspectives on MAGICAL: A Silicon-Proven Open-Source Analog IC Layout System. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2022**, 1-1 | 3.5 | |
| 150 | Light in AI: Toward Efficient Neurocomputing with Optical Neural Networks -A Tutorial. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2022**, 1-1 | 3.5 | |
| 149 | MLCAD: A Survey of Research in Machine Learning for CAD Keynote Paper. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2021**, 1-1 | 2.5 | 1 |
| 148 | Toward High-Speed and Energy-Efficient Computing: A WDM-Based Scalable On-Chip Silicon Integrated Optical Comparator. *Laser and Photonics Reviews*, **2021**, 15, 2000275 | 8.3 | 1 |
| 147 | GAN-SRAF: Subresolution Assist Feature Generation Using Generative Adversarial Networks. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2021**, 40, 373-385 | 2.5 | 2 |
| 146 | DREAMPlace: Deep Learning Toolkit-Enabled GPU Acceleration for Modern VLSI Placement. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2021**, 40, 748-761 | 2.5 | 16 |
| 145 | MAGICAL: An Open- Source Fully Automated Analog IC Layout System from Netlist to GDSII. *IEEE Design and Test*, **2021**, 38, 19-26 | 1.4 | 5 |
| 144 | . *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2021**, 40, 1796-1809 | 2.5 | 4 |
| 143 | An Efficient Analog Circuit Sizing Method Based on Machine Learning Assisted Global Optimization. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2021**, 1-1 | 2.5 | 2 |
| 142 | O2NN: Optical Neural Networks with Differential Detection-Enabled Optical Operands **2021**, | | 2 |
| 141 | SqueezeLight: Towards Scalable Optical Neural Networks with Multi-Operand Ring Resonators **2021**, | | 3 |
| 140 | Identification of TBX15 as an adipose master trans regulator of abdominal obesity genes. *Genome Medicine*, **2021**, 13, 123 | 14.4 | 2 |
| 139 | An Efficient Automatic Structure Design Method of Silicon-on-Insulator Lateral Power Device Considering RESURF Constraint. *IEEE Transactions on Electron Devices*, **2021**, 68, 4593-4597 | 2.9 | 1 |
| 138 | elfPlace: Electrostatics-based Placement for Large-Scale Heterogeneous FPGAs. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2021**, 1-1 | 2.5 | 1 |
| 137 | Electronic-photonic arithmetic logic unit for high-speed computing. *Nature Communications*, **2020**, 11, 2154 | 17.4 | 35 |

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| 136 | 9.5 A 13.5b-ENOB Second-Order Noise-Shaping SAR with PVT-Robust Closed-Loop Dynamic Amplifier **2020**, | | 11 |
| 135 | ABCDPlace: Accelerated Batch-Based Concurrent Detailed Placement on Multithreaded CPUs and GPUs. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2020**, 39, 5083-5096 | 2.5 | 12 |
| 134 | ROQ: A Noise-Aware Quantization Scheme Towards Robust Optical Neural Networks with Low-bit Controls **2020**, | | 3 |
| 133 | An Energy-Efficient Time-Domain Incremental Zoom Capacitance-to-Digital Converter. *IEEE Journal of Solid-State Circuits*, **2020**, 55, 3064-3075 | 5.5 | 5 |
| 132 | Powernet: SOI Lateral Power Device Breakdown Prediction With Deep Neural Networks. *IEEE Access*, **2020**, 8, 25372-25382 | 3.5 | 15 |
| 131 | Virtual-Tile-Based Flip-Flop Alignment Methodology for Clock Network Power Optimization. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2020**, 28, 1256-1268 | 2.6 | 0 |
| 130 | TimingCamouflage+: Netlist Security Enhancement With Unconventional Timing. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2020**, 39, 4482-4495 | 2.5 | 1 |
| 129 | Report on the 38th ACM/IEEE International Conference on Computer-Aided Design (ICCAD 2019). *IEEE Design and Test*, **2020**, 37, 121-122 | 1.4 | |
| 128 | Towards Area-Efficient Optical Neural Networks: An FFT-based Architecture **2020**, | | 13 |
| 127 | S3DET: Detecting System Symmetry Constraints for Analog Circuits with Graph Similarity **2020**, | | 2 |
| 126 | High-Definition Routing Congestion Prediction for Large-Scale FPGAs **2020**, | | 11 |
| 125 | OpenMPL: An Open Source Layout Decomposer. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2020**, 1-1 | 2.5 | 2 |
| 124 | TEMPO: Fast Mask Topography Effect Modeling with Deep Learning **2020**, | | 4 |
| 123 | Wavelength-division-multiplexing (WDM)-based integrated electronic–photonic switching network (EPSN) for high-speed data processing and transportation. *Nanophotonics*, **2020**, 9, 4579-4588 | 6.3 | 6 |
| 122 | Practical Split Manufacturing Optimization **2020**, 9-38 | | |
| 121 | Compact Design of On-chip Elman Optical Recurrent Neural Network **2020**, | | 4 |
| 120 | DREAMPlace 3.0 **2020**, | | 2 |
| 119 | An Efficient Training Framework for Reversible Neural Architectures. *Lecture Notes in Computer Science*, **2020**, 275-289 | 0.9 | |

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| 118 | DREAMPlace 2.0: Open-Source GPU-Accelerated Global and Detailed Placement for Large-Scale VLSI Designs **2020**, | | 2 |
| 117 | Integrated WDM-based Optical Comparator for High-speed Computing **2020**, | | 2 |
| 116 | . *IEEE Journal of Solid-State Circuits*, **2020**, 55, 1011-1022 | 5.5 | 25 |
| 115 | A 0.025-mm2 0.8-V 78.5-dB SNDR VCO-Based Sensor Readout Circuit in a Hybrid PLL- $DeltaSigma$ M Structure. *IEEE Journal of Solid-State Circuits*, **2020**, 55, 666-679 | 5.5 | 19 |
| 114 | Analysis of Microresonator-Based Logic Gate for High-Speed Optical Computing in Integrated Photonics. *IEEE Journal of Selected Topics in Quantum Electronics*, **2020**, 26, 1-8 | 3.8 | 5 |
| 113 | Sequential Logic and Pipelining in Chip-Based Electronic-Photonic Digital Computing. *IEEE Photonics Journal*, **2020**, 12, 1-11 | 1.8 | 2 |
| 112 | FLOPS: EFficient On-Chip Learning for OPtical Neural Networks Through Stochastic Zeroth-Order Optimization **2020**, | | 5 |
| 111 | Closing the Design Loop: Bayesian Optimization Assisted Hierarchical Analog Layout Synthesis **2020**, | | 4 |
| 110 | A 13.5-ENOB, 107-W Noise-Shaping SAR ADC With PVT-Robust Closed-Loop Dynamic Amplifier. *IEEE Journal of Solid-State Circuits*, **2020**, 55, 3248-3259 | 5.5 | 20 |
| 109 | Automatic Selection of Structure Parameters of Silicon on Insulator Lateral Power Device Using Bayesian Optimization. *IEEE Electron Device Letters*, **2020**, 41, 1288-1291 | 4.4 | 6 |
| 108 | Semisupervised Hotspot Detection With Self-Paced Multitask Learning. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2020**, 39, 1511-1523 | 2.5 | 7 |
| 107 | An OTA-Less Second-Order VCO-Based CT $DeltaSigma$ Modulator Using an Inherent Passive Integrator and Capacitive Feedback. *IEEE Journal of Solid-State Circuits*, **2020**, 55, 1337-1350 | 5.5 | 3 |
| 106 | GAN-SRAF **2019**, | | 9 |
| 105 | IP Protection and Supply Chain Security through Logic Obfuscation. *ACM Transactions on Design Automation of Electronic Systems*, **2019**, 24, 1-36 | 1.5 | 24 |
| 104 | Rethinking Sparsity in Performance Modeling for Analog and Mixed Circuits using Spike and Slab Models **2019**, | | 3 |
| 103 | LithoGAN **2019**, | | 21 |
| 102 | DREAMPlace **2019**, | | 16 |
| 101 | Reverse gene-environment interaction approach to identify variants influencing body-mass index in humans. *Nature Metabolism*, **2019**, 1, 630-642 | 14.6 | 6 |

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| 100 | A New Physical Understanding of Lateral Step Doping Technique via Effective Concentration Profile Concept. *IEEE Transactions on Electron Devices*, **2019**, 66, 2353-2358 | 2.9 | 5 |
| 99 | Device Layer-Aware Analytical Placement for Analog Circuits **2019**, | | 2 |
| 98 | Hardware-software co-design of slimmed optical neural networks **2019**, | | 11 |
| 97 | Simultaneous Placement and Clock Tree Construction for Modern FPGAs **2019**, | | 2 |
| 96 | . *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2019**, 38, 1147-1160 | 2.5 | 4 |
| 95 | On the Approximation Resiliency of Logic Locking and IC Camouflaging Schemes. *IEEE Transactions on Information Forensics and Security*, **2019**, 14, 347-359 | 8 | 23 |
| 94 | Data Efficient Lithography Modeling With Transfer Learning and Active Data Selection. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2019**, 38, 1900-1913 | 2.5 | 12 |
| 93 | A Practical Split Manufacturing Framework for Trojan Prevention via Simultaneous Wire Lifting and Cell Insertion. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2019**, 38, 1585-1598 | 2.5 | 8 |
| 92 | WellGAN **2019**, | | 13 |
| 91 | On the Impossibility of Approximation-Resilient Circuit Locking **2019**, | | 12 |
| 90 | Exploiting Wavelength Division Multiplexing for Optical Logic Synthesis **2019**, | | 2 |
| 89 | MAGICAL: Toward Fully Automated Analog IC Layout Leveraging Human and Machine Intelligence: Invited Paper **2019**, | | 12 |
| 88 | Lithography hotspot detection using a double inception module architecture. *Journal of Micro/ Nanolithography, MEMS, and MOEMS*, **2019**, 18, 1 | 0.7 | 7 |
| 87 | SoulNet: ultrafast optical source optimization utilizing generative neural networks for advanced lithography. *Journal of Micro/ Nanolithography, MEMS, and MOEMS*, **2019**, 18, 1 | 0.7 | 1 |
| 86 | Machine Learning in Physical Verification, Mask Synthesis, and Physical Design **2019**, 95-115 | | 1 |
| 85 | GeniusRoute: A New Analog Routing Paradigm Using Generative Neural Network Guidance **2019**, | | 11 |
| 84 | elfPlace: Electrostatics-based Placement for Large-Scale Heterogeneous FPGAs **2019**, | | 6 |
| 83 | KC2: Key-Condition Crunching for Fast Sequential Circuit Deobfuscation **2019**, | | 24 |

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| 82 | Power and Accuracy Co-Optimization of an Optical Full Adder via Optimization Algorithms **2019**, | | 1 |
| 81 | A New Paradigm for FPGA Placement Without Explicit Packing. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2019**, 38, 2113-2126 | 2.5 | 3 |
| 80 | A New Low Turn-Off Loss SOI Lateral Insulated Gate Bipolar Transistor With Buried Variation of Lateral Doping Layer. *IEEE Journal of the Electron Devices Society*, **2019**, 7, 62-69 | 2.3 | 4 |
| 79 | Provably Secure Camouflaging Strategy for IC Protection. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2019**, 38, 1399-1412 | 2.5 | 17 |
| 78 | Integration of human adipocyte chromosomal interactions with adipose gene expression prioritizes obesity-related genes from GWAS. *Nature Communications*, **2018**, 9, 1512 | 17.4 | 41 |
| 77 | A New Physical Insight for the 3-D-Layout-Induced Cylindrical Breakdown in Lateral Power Devices on SOI Substrate. *IEEE Transactions on Electron Devices*, **2018**, 65, 1843-1848 | 2.9 | 4 |
| 76 | MrDP: Multiple-Row Detailed Placement of Heterogeneous-Sized Cells for Advanced Nodes. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2018**, 37, 1237-1250 | 2.5 | 9 |
| 75 | Thermal Stress and Reliability Analysis of TSV-Based 3-D ICs With a Novel Adaptive Strategy Finite Element Method. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2018**, 26, 1312-1325 | 2.6 | 5 |
| 74 | Effective Doping Concentration Theory: A New Physical Insight for the Double-RESURF Lateral Power Devices on SOI Substrate. *IEEE Transactions on Electron Devices*, **2018**, 65, 648-654 | 2.9 | 17 |
| 73 | A Novel Variation of Lateral Doping Technique in SOI LDMOS With Circular Layout. *IEEE Transactions on Electron Devices*, **2018**, 65, 1447-1452 | 2.9 | 14 |
| 72 | Comparison of microrings and microdisks for high-speed optical modulation in silicon photonics. *Applied Physics Letters*, **2018**, 112, 111108 | 3.4 | 18 |
| 71 | Logic synthesis for energy-efficient photonic integrated circuits **2018**, | | 5 |
| 70 | TILA-S: Timing-Driven Incremental Layer Assignment Avoiding Slew Violations. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2018**, 37, 231-244 | 2.5 | 7 |
| 69 | UTPlaceF: A Routability-Driven FPGA Placer With Physical and Congestion Aware Packing. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2018**, 37, 869-882 | 2.5 | 19 |
| 68 | Silicon microdisk-based full adders for optical computing. *Optics Letters*, **2018**, 43, 983-986 | 3 | 31 |
| 67 | An Improved Domain Decomposition Method for Drop Impact Reliability Analysis of 3-D ICs. *IEEE Transactions on Components, Packaging and Manufacturing Technology*, **2018**, 8, 1788-1799 | 1.7 | 2 |
| 66 | TimingCamouflage: Improving circuit security against counterfeiting by unconventional timing **2018**, | | 17 |
| 65 | Subresolution Assist Feature Generation With Supervised Data Learning. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2018**, 37, 1225-1236 | 2.5 | 9 |

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| 64 | Cut Redistribution and Insertion for Advanced 1-D Layout Design via Network Flow Optimization. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2018**, 26, 1613-1626 | 2.6 | |
| 63 | Automated logic synthesis for electro-optic logic-based integrated optical computing. *Optics Express*, **2018**, 26, 28002-28012 | 3.3 | 17 |
| 62 | Interlayer Cooling Network Design for High-Performance 3D ICs Using Channel Patterning and Pruning. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2018**, 37, 770-781 | 2.5 | 6 |
| 61 | Machine Learning for Yield Learning and Optimization **2018**, | | 8 |
| 60 | TimingSAT: Decamouflaging Timing-based Logic Obfuscation **2018**, | | 8 |
| 59 | Effective Concentration Profile: Mechanism of Gate Field-Plate Assistant Effect in SOI Lateral Power Devices. *IEEE Transactions on Electron Devices*, **2018**, 65, 4476-4482 | 2.9 | 6 |
| 58 | GDP: GPU accelerated Detailed Placement **2018**, | | 7 |
| 57 | Role of Shape Factor in Forming Surface Electric Field Basin in RESURF Lateral Power Devices and its Optimization Design. *IEEE Journal of the Electron Devices Society*, **2018**, 6, 1147-1153 | 2.3 | 5 |
| 56 | A 13-ENOB Second-Order Noise-Shaping SAR ADC Realizing Optimized NTF Zeros Using the Error-Feedback Structure. *IEEE Journal of Solid-State Circuits*, **2018**, 53, 3484-3496 | 5.5 | 50 |
| 55 | UTPlaceF 2.0. *ACM Transactions on Design Automation of Electronic Systems*, **2018**, 23, 1-23 | 1.5 | 6 |
| 54 | Layout Synthesis for Topological Quantum Circuits With 1-D and 2-D Architectures. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2018**, 37, 1574-1587 | 2.5 | 4 |
| 53 | Triple Patterning Aware Detailed Placement Toward Zero Cross-Row Middle-of-Line Conflict. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2017**, 36, 1140-1152 | 2.5 | 7 |
| 52 | Redundant Local-Loop Insertion for Unidirectional Routing. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2017**, 36, 1113-1125 | 2.5 | 1 |
| 51 | Triple/quadruple patterning layout decomposition via linear programming and iterative rounding. *Journal of Micro/ Nanolithography, MEMS, and MOEMS*, **2017**, 16, 023507 | 0.7 | 3 |
| 50 | Incremental Layer Assignment Driven by an External Signoff Timing Engine. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2017**, 36, 1126-1139 | 2.5 | 3 |
| 49 | High Performance Dummy Fill Insertion With Coupling and Uniformity Constraints. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2017**, 36, 1532-1544 | 2.5 | 5 |
| 48 | Cyclic Obfuscation for Creating SAT-Unresolvable Circuits **2017**, | | 78 |
| 47 | AppSAT: Approximately deobfuscating integrated circuits **2017**, | | 131 |

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| 46 | Optical computing on silicon-on-insulator-based photonic integrated circuits **2017**, | | 5 |
| 45 | Polynomial Time Algorithm for Area and Power Efficient Adder Synthesis in High-Performance Designs. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2016**, 35, 820-831 | 2.5 | 5 |
| 44 | A Novel 3-D Analytical Method for Curvature Effect-Induced Electric Field Crowding in SOI Lateral Power Device. *IEEE Transactions on Electron Devices*, **2016**, 63, 4359-4365 | 2.9 | 8 |
| 43 | Provably secure camouflaging strategy for IC protection **2016**, | | 49 |
| 42 | Self-Aligned Double Patterning Aware Pin Access and Standard Cell Layout Co-Optimization. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2015**, 34, 699-712 | 2.5 | 23 |
| 41 | Methodology for Standard Cell Compliance and Detailed Placement for Triple Patterning Lithography. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2015**, 34, 726-739 | 2.5 | 21 |
| 40 | Layout Decomposition for Triple Patterning Lithography. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2015**, 34, 433-446 | 2.5 | 32 |
| 39 | Clock Tree Resynthesis for Multi-Corner Multi-Mode Timing Closure. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2015**, 34, 589-602 | 2.5 | 12 |
| 38 | Polynomial time algorithm for area and power efficient adder synthesis in high-performance designs **2015**, | | 5 |
| 37 | Pushing multiple patterning in sub-10nm **2015**, | | 20 |
| 36 | CSL: Coordinated and scalable logic synthesis techniques for effective NBTI reduction **2015**, | | 1 |
| 35 | Towards Optimal Performance-Area Trade-Off in Adders by Synthesis of Parallel Prefix Structures. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2014**, 33, 1517-1530 | 2.5 | 12 |
| 34 | Reliability Aware Gate Sizing Combating NBTI and Oxide Breakdown **2014**, | | 6 |
| 33 | Evolving challenges and techniques for nanometer SoC clock network synthesis **2014**, | | 5 |
| 32 | Electromigration Study for Multiscale Power/Ground Vias in TSV-Based 3-D ICs. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2014**, 33, 1873-1885 | 2.5 | 11 |
| 31 | Triple patterning lithography layout decomposition using end-cutting. *Journal of Micro/Nanolithography, MEMS, and MOEMS*, **2014**, 14, 011002 | 0.7 | 6 |
| 30 | An accurate semi-analytical framework for full-chip TSV-induced stress modeling **2013**, | | 1 |
| 29 | Design for Manufacturing With Emerging Nanolithography. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2013**, 32, 1453-1472 | 2.5 | 69 |

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| 28 | Chemical-Mechanical Polishing-Aware Application-Specific 3D NoC Design. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2013**, 32, 940-951 | 2.5 | |
| 27 | Impact of Mechanical Stress on the Full Chip Timing for Through-Silicon-Via-based 3-D ICs. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2013**, 32, 905-917 | 2.5 | 10 |
| 26 | Skew Management of NBTI Impacted Gated Clock Trees. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2013**, 32, 918-927 | 2.5 | 4 |
| 25 | A high-performance triple patterning layout decomposer with balanced density **2013**, | | 24 |
| 24 | E-Beam Lithography Stencil Planning and Optimization With Overlapped Characters. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2012**, 31, 167-179 | 2.5 | 24 |
| 23 | TSV Stress-Aware Full-Chip Mechanical Reliability Analysis and Optimization for 3-D IC. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2012**, 31, 1194-1207 | 2.5 | 30 |
| 22 | UNISM: Unified Scheduling and Mapping for General Networks on Chip. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2012**, 20, 1496-1509 | 2.6 | 40 |
| 21 | Robust and resilient designs from the bottom-up: Technology, CAD, circuit, and system issues **2012**, | | 9 |
| 20 | A Voltage-Frequency Island Aware Energy Optimization Framework for Networks-on-Chip. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, **2011**, 1, 420-432 | 5.2 | 23 |
| 19 | Application-Aware NoC Design for Efficient SDRAM Access. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2011**, 30, 1521-1533 | 2.5 | 10 |
| 18 | Electromigration modeling and full-chip reliability analysis for BEOL interconnect in TSV-based 3D ICs **2011**, | | 23 |
| 17 | CELONCEL: Effective design technique for 3-D monolithic integration targeting high performance integrated circuits **2011**, | | 30 |
| 16 | A fast simulation framework for full-chip thermo-mechanical stress and reliability analysis of through-silicon-via based 3D ICs **2011**, | | 9 |
| 15 | Modeling of electromigration in through-silicon-via based 3D IC **2011**, | | 33 |
| 14 | TSV stress aware timing analysis with applications to 3D-IC layout optimization **2010**, | | 72 |
| 13 | Stress-driven 3D-IC placement with TSV keep-out zone and regularity study **2010**, | | 47 |
| 12 | A3MAP: Architecture-Aware Analytic Mapping for Networks-on-Chip **2010**, | | 9 |
| 11 | . *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2010**, 29, 185-196 | 2.5 | 34 |

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| 10 | Stress Aware Layout Optimization Leveraging Active Area Dependent Mobility Enhancement. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2010**, 29, 1533-1545 | 2.5 | 2 |
| 9 | Voltage and frequency island optimizations for many-core/networks-on-chip designs **2010**, | | 4 |
| 8 | A High-Performance Droplet Routing Algorithm for Digital Microfluidic Biochips. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2008**, 27, 1714-1724 | 2.5 | 87 |
| 7 | DPlace2.0: A stable and efficient analytical placement based on diffusion **2008**, | | 2 |
| 6 | Fast Substrate Noise Aware Floorplanning for Mixed Signal SOC Designs. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2008**, 16, 1713-1717 | 2.6 | 0 |
| 5 | A Voltage-Frequency Island aware energy optimization framework for networks-on-chip **2008**, | | 4 |
| 4 | Layout Level Timing Optimization by Leveraging Active Area Dependent Mobility of Strained-Silicon Devices **2008**, | | 4 |
| 3 | A novel intensity based optical proximity correction algorithm with speedup in lithography simulation. *IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers* , **2007**, | | 4 |
| 2 | TIP-OPC: a new topological invariant paradigm for pixel based optical proximity correction. *IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers*, **2007**, | | 1 |
| 1 | Diffusion-Based Placement Migration With Application on Legalization. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2007**, 26, 2158-2172 | 2.5 | 3 |