David Z Pan

List of Publications by Year
in descending order

172 papers	3,655 citations	218381 26 h-index	276539 41 g-index
176 all docs	176 docs citations	176 times ranked	2152 citing authors

#	Article	IF	Citations
1	AppSAT: Approximately deobfuscating integrated circuits. , 2017, , .		215
2	A High-Performance Droplet Routing Algorithm for Digital Microfluidic Biochips. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 1714-1724.	1.9	119
3	Cyclic Obfuscation for Creating SAT-Unresolvable Circuits. , 2017, , .		116
4	An Energy-Efficient Comparator With Dynamic Floating Inverter Amplifier. IEEE Journal of Solid-State Circuits, 2020, 55, 1011-1022.	3.5	107
5	Design for Manufacturing With Emerging Nanolithography. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2013, 32, 1453-1472.	1.9	100
6	TSV stress aware timing analysis with applications to 3D-IC layout optimization. , 2010, , .		90
7	Electronic-photonic arithmetic logic unit for high-speed computing. Nature Communications, 2020, 11, 2154.	5.8	84
8	A 13-ENOB Second-Order Noise-Shaping SAR ADC Realizing Optimized NTF Zeros Using the Error-Feedback Structure. IEEE Journal of Solid-State Circuits, 2018, 53, 3484-3496.	3.5	80
9	Integration of human adipocyte chromosomal interactions with adipose gene expression prioritizes obesity-related genes from GWAS. Nature Communications, 2018, 9, 1512.	5.8	75
10	Provably secure camouflaging strategy for IC protection. , 2016, , .		73
11	IP Protection and Supply Chain Security through Logic Obfuscation. ACM Transactions on Design Automation of Electronic Systems, 2019, 24, 1-36.	1.9	61
12	Stress-driven 3D-IC placement with TSV keep-out zone and regularity study. , 2010, , .		60
13	KC2: Key-Condition Crunching for Fast Sequential Circuit Deobfuscation. , 2019, , .		59
14	Double Patterning Layout Decomposition for Simultaneous Conflict and Stitch Minimization. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2010, 29, 185-196.	1.9	57
15	DREAMPlace. , 2019, , .		56
16	Layout Decomposition for Triple Patterning Lithography. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2015, 34, 433-446.	1.9	54
17	DREAMPlace: Deep Learning Toolkit-Enabled GPU Acceleration for Modern VLSI Placement. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 748-761.	1.9	51
18	UNISM: Unified Scheduling and Mapping for General Networks on Chip. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2012, 20, 1496-1509.	2.1	49

#	Article	IF	Citations
19	LithoGAN. , 2019, , .		48
20	Modeling of electromigration in through-silicon-via based 3D IC. , 2011, , .		47
21	UTPlaceF: A Routability-Driven FPGA Placer With Physical and Congestion Aware Packing. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 869-882.	1.9	47
22	Silicon microdisk-based full adders for optical computing. Optics Letters, 2018, 43, 983.	1.7	47
23	A 13.5-ENOB, 107-Î¼W Noise-Shaping SAR ADC With PVT-Robust Closed-Loop Dynamic Amplifier. IEEE Journal of Solid-State Circuits, 2020, 55, 3248-3259.	3.5	47
24	On the Approximation Resiliency of Logic Locking and IC Camouflaging Schemes. IEEE Transactions on Information Forensics and Security, 2019, 14, 347-359.	4.5	46
25	TSV Stress-Aware Full-Chip Mechanical Reliability Analysis and Optimization for 3-D IC. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2012, 31, 1194-1207.	1.9	44
26	WellGAN. , 2019, , .		42
27	GeniusRoute: A New Analog Routing Paradigm Using Generative Neural Network Guidance. , 2019, , .		39
28	MAGICAL: Toward Fully Automated Analog IC Layout Leveraging Human and Machine Intelligence: Invited Paper. , 2019, , .		39
29	Self-Aligned Double Patterning Aware Pin Access and Standard Cell Layout Co-Optimization. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2015, 34, 699-712.	1.9	38
30	Powernet: SOI Lateral Power Device Breakdown Prediction With Deep Neural Networks. IEEE Access, 2020, 8, 25372-25382.	2.6	38
31	A 0.025-mm² 0.8-V 78.5-dB SNDR VCO-Based Sensor Readout Circuit in a Hybrid PLL-$DeltaSigma$ M Structure. IEEE Journal of Solid-State Circuits, 2020, 55, 666-679.	3.5	37
32	CELONCEL: Effective design technique for 3-D monolithic integration targeting high performance integrated circuits. , 2011, , .		36
33	A high-performance triple patterning layout decomposer with balanced density. , 2013, , .		35
34	High-Definition Routing Congestion Prediction for Large-Scale FPGAs. , 2020, , .		35
35	Methodology for Standard Cell Compliance and Detailed Placement for Triple Patterning Lithography. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2015, 34, 726-739.	1.9	33
36	Towards Area-Efficient Optical Neural Networks: An FFT-based Architecture. , 2020, , .		33

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37	E-Beam Lithography Stencil Planning and Optimization With Overlapped Characters. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2012, 31, 167-179.	1.9	32
38	Provably Secure Camouflaging Strategy for IC Protection. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 1399-1412.	1.9	32
39	9.5 A 13.5b-ENOB Second-Order Noise-Shaping SAR with PVT-Robust Closed-Loop Dynamic Amplifier. , 2020, , .		31
40	A Voltage-Frequency Island Aware Energy Optimization Framework for Networks-on-Chip. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2011, 1, 420-432.	2.7	30
41	TimingCamouflage: Improving circuit security against counterfeiting by unconventional timing. , 2018, , .		29
42	Data Efficient Lithography Modeling With Transfer Learning and Active Data Selection. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 1900-1913.	1.9	29
43	Electromigration modeling and full-chip reliability analysis for BEOL interconnect in TSV-based 3D ICs. , 2011, , .		28
44	On the Impossibility of Approximation-Resilient Circuit Locking. , 2019, , .		28
45	Towards Optimal Performance-Area Trade-Off in Adders by Synthesis of Parallel Prefix Structures. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2014, 33, 1517-1530.	1.9	27
46	Comparison of microrings and microdisks for high-speed optical modulation in silicon photonics. Applied Physics Letters, 2018, 112, 111108.	1.5	27
47	ABCDPlace: Accelerated Batch-Based Concurrent Detailed Placement on Multithreaded CPUs and GPUs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 5083-5096.	1.9	27
48	Automated logic synthesis for electro-optic logic-based integrated optical computing. Optics Express, 2018, 26, 28002.	1.7	27
49	Clock Tree Resynthesis for Multi-Corner Multi-Mode Timing Closure. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2015, 34, 589-602.	1.9	26
50	Pushing multiple patterning in sub-10nm. , 2015, , .		26
51	Hardware-software co-design of slimmed optical neural networks. , 2019, , .		25
52	Effective Doping Concentration Theory: A New Physical Insight for the Double-RESURF Lateral Power Devices on SOI Substrate. IEEE Transactions on Electron Devices, 2018, 65, 648-654.	1.6	23
53	MAGICAL: An Open- Source Fully Automated Analog IC Layout System from Netlist to GDSII. IEEE Design and Test, 2021, 38, 19-26.	1.1	23
54	Identification of TBX15 as an adipose master trans regulator of abdominal obesity genes. Genome Medicine, 2021, 13, 123.	3.6	23

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55	MLCAD: A Survey of Research in Machine Learning for CAD Keynote Paper. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 3162-3181.	1.9	22
56	MrDP: Multiple-Row Detailed Placement of Heterogeneous-Sized Cells for Advanced Nodes. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 1237-1250.	1.9	21
57	A Novel Variation of Lateral Doping Technique in SOI LDMOS With Circular Layout. IEEE Transactions on Electron Devices, 2018, 65, 1447-1452.	1.6	21
58	elfPlace: Electrostatics-based Placement for Large-Scale Heterogeneous FPGAs. , 2019, , .		19
59	An Energy-Efficient Time-Domain Incremental Zoom Capacitance-to-Digital Converter. IEEE Journal of Solid-State Circuits, 2020, 55, 3064-3075.	3.5	19
60	S³DET: Detecting System Symmetry Constraints for Analog Circuits with Graph Similarity. , 2020, , .		19
61	A New Paradigm for FPGA Placement Without Explicit Packing. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 2113-2126.	1.9	18
62	An Efficient Analog Circuit Sizing Method Based on Machine Learning Assisted Global Optimization. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 1209-1221.	1.9	18
63	UTPlaceF 2.0. ACM Transactions on Design Automation of Electronic Systems, 2018, 23, 1-23.	1.9	17
64	GAN-SRAF. , 2019, , .		17
65	Wavelength-division-multiplexing (WDM)-based integrated electronicâ€“photonic switching network (EPSN) for high-speed data processing and transportation. Nanophotonics, 2020, 9, 4579-4588.	2.9	16
66	Subresolution Assist Feature Generation With Supervised Data Learning. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 1225-1236.	1.9	15
67	Device Layer-Aware Analytical Placement for Analog Circuits. , 2019, , .		15
68	Impact of Mechanical Stress on the Full Chip Timing for Through-Silicon-Via-based 3-D ICs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2013, 32, 905-917.	1.9	14
69	Polynomial Time Algorithm for Area and Power Efficient Adder Synthesis in High-Performance Designs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, 35, 820-831.	1.9	14
70	TILA-S: Timing-Driven Incremental Layer Assignment Avoiding Slew Violations. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 231-244.	1.9	14
71	Reverse geneâ€“environment interaction approach to identify variants influencing body-mass index in humans. Nature Metabolism, 2019, 1, 630-642.	5.1	14
72	Semisupervised Hotspot Detection With Self-Paced Multitask Learning. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 1511-1523.	1.9	14

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73	Automatic Selection of Structure Parameters of Silicon on Insulator Lateral Power Device Using Bayesian Optimization. IEEE Electron Device Letters, 2020, 41, 1288-1291.	2.2	14
74	SqueezeLight: Towards Scalable Optical Neural Networks with Multi-Operand Ring Resonators. , 2021, , .		14
75	Machine Learning for Yield Learning and Optimization. , 2018, , .		13
76	Toward Hardware-Efficient Optical Neural Networks: Beyond FFT Architecture via Joint Learnability. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 1796-1809.	1.9	13
77	Application-Aware NoC Design for Efficient SDRAM Access. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2011, 30, 1521-1533.	1.9	12
78	Robust and resilient designs from the bottom-up: Technology, CAD, circuit, and system issues. , 2012, , .		12
79	Electromigration Study for Multiscale Power/Ground Vias in TSV-Based 3-D ICs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2014, 33, 1873-1885.	1.9	12
80	Triple patterning lithography layout decomposition using end-cutting. Journal of Micro/Nanolithography, MEMS, and MOEMS, 2014, 14, 011002.	1.0	12
81	Logic synthesis for energy-efficient photonic integrated circuits. , 2018, , .		12
82	TimingSAT: Decamouflaging Timing-based Logic Obfuscation. , 2018, , .		12
83	A Practical Split Manufacturing Framework for Trojan Prevention via Simultaneous Wire Lifting and Cell Insertion. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 1585-1598.	1.9	12
84	Closing the Design Loop: Bayesian Optimization Assisted Hierarchical Analog Layout Synthesis. , 2020, , .		12
85	SHIELDeNN: Online Accelerated Framework for Fault-Tolerant Deep Neural Network Architectures. , 2020, , .		12
86	Lithography hotspot detection using a double inception module architecture. Journal of Micro/Nanolithography, MEMS, and MOEMS, 2019, 18, 1.	1.0	12
87	Diffusion-Based Placement Migration With Application on Legalization. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2007, 26, 2158-2172.	1.9	11
88	A3MAP: Architecture-Aware Analytic Mapping for Networks-on-Chip. , 2010, , .		11
89	A fast simulation framework for full-chip thermo-mechanical stress and reliability analysis of through-silicon-via based 3D ICs. , 2011, , .		11
90	GDP: GPU accelerated Detailed Placement. , 2018, , .		11

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91	An OTA-Less Second-Order VCO-Based CT $DeltaSigma$ Modulator Using an Inherent Passive Integrator and Capacitive Feedback. IEEE Journal of Solid-State Circuits, 2020, 55, 1337-1350.	3.5	11
92	FLOPS: EFficient On-Chip Learning for OPtical Neural Networks Through Stochastic Zeroth-Order Optimization. , 2020, , .		11
93	GAN-SRAF: Subresolution Assist Feature Generation Using Generative Adversarial Networks. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 373-385.	1.9	11
94	Toward Highâ€Speed and Energyâ€Efficient Computing: A WDMâ€Based Scalable Onâ€Chip Silicon Integrated Optical Comparator. Laser and Photonics Reviews, 2021, 15, 2000275.	4.4	11
95	elfPlace: Electrostatics-Based Placement for Large-Scale Heterogeneous FPGAs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 155-168.	1.9	11
96	TEMPO: Fast Mask Topography Effect Modeling with Deep Learning. , 2020, , .		11
97	DREAMPlace 3.0. , 2020, , .		11
98	Reliability Aware Gate Sizing Combating NBTI and Oxide Breakdown. , 2014, , .		10
99	High Performance Dummy Fill Insertion With Coupling and Uniformity Constraints. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 1532-1544.	1.9	10
100	Simultaneous Placement and Clock Tree Construction for Modern FPGAs. , 2019, , .		10
101	Identification of 90 NAFLD GWAS loci and establishment of NAFLD PRS and causal role of NAFLD in coronary artery disease. Human Genetics and Genomics Advances, 2022, 3, 100056.	1.0	10
102	Triple Patterning Aware Detailed Placement Toward Zero Cross-Row Middle-of-Line Conflict. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 1140-1152.	1.9	9
103	Analysis of Microresonator-Based Logic Gate for High-Speed Optical Computing in Integrated Photonics. IEEE Journal of Selected Topics in Quantum Electronics, 2020, 26, 1-8.	1.9	9
104	ROQ: A Noise-Aware Quantization Scheme Towards Robust Optical Neural Networks with Low-bit Controls. , 2020, , .		9
105	A Novel 3-D Analytical Method for Curvature Effect-Induced Electric Field Crowding in SOI Lateral Power Device. IEEE Transactions on Electron Devices, 2016, 63, 4359-4365.	1.6	8
106	Triple/quadruple patterning layout decomposition via linear programming and iterative rounding. Journal of Micro/ Nanolithography, MEMS, and MOEMS, 2017, 16, 023507.	1.0	8
107	Thermal Stress and Reliability Analysis of TSV-Based 3-D ICs With a Novel Adaptive Strategy Finite Element Method. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 1312-1325.	2.1	8
108	Interlayer Cooling Network Design for High-Performance 3D ICs Using Channel Patterning and Pruning. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 770-781.	1.9	8

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109	Effective Concentration Profile: Mechanism of Gate Field-Plate Assistant Effect in SOI Lateral Power Devices. IEEE Transactions on Electron Devices, 2018, 65, 4476-4482.	1.6	8
110	Breakdown Voltage Prediction of SOI Lateral Power Device Using Deep Neural Network. , 2019, , .		8
111	Optical computing on silicon-on-insulator-based photonic integrated circuits. , 2017, , .		7
112	Layout Synthesis for Topological Quantum Circuits With 1-D and 2-D Architectures. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 1574-1587.	1.9	7
113	Synergistic Topology Generation and Route Synthesis for On-Chip Performance-Critical Signal Groups. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 1147-1160.	1.9	7
114	Exploiting Wavelength Division Multiplexing for Optical Logic Synthesis. , 2019, , .		7
115	O2NN: Optical Neural Networks with Differential Detection-Enabled Optical Operands. , 2021, , .		7
116	OpenMPL: An Open-Source Layout Decomposer. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 2331-2344.	1.9	7
117	Compact Design of On-chip Elman Optical Recurrent Neural Network. , 2020, , .		7
118	Skew Management of NBTI Impacted Gated Clock Trees. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2013, 32, 918-927.	1.9	6
119	A New Physical Insight for the 3-D-Layout-Induced Cylindrical Breakdown in Lateral Power Devices on SOI Substrate. IEEE Transactions on Electron Devices, 2018, 65, 1843-1848.	1.6	6
120	Directed self-assembly for advanced chips. Nature Electronics, 2018, 1, 530-531.	13.1	6
121	A New Physical Understanding of Lateral Step Doping Technique via Effective Concentration Profile Concept. IEEE Transactions on Electron Devices, 2019, 66, 2353-2358.	1.6	6
122	A New Low Turn-Off Loss SOI Lateral Insulated Gate Bipolar Transistor With Buried Variation of Lateral Doping Layer. IEEE Journal of the Electron Devices Society, 2019, 7, 62-69.	1.2	6
123	DREAMPlace 2.0: Open-Source GPU-Accelerated Global and Detailed Placement for Large-Scale VLSI Designs. , 2020, , .		6
124	Layout Level Timing Optimization by Leveraging Active Area Dependent Mobility of Strained-Silicon Devices. , 2008, , .		5
125	Evolving challenges and techniques for nanometer SoC clock network synthesis. , 2014, , .		5
126	Polynomial time algorithm for area and power efficient adder synthesis in high-performance designs. , 2015, , .		5

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127	Role of Shape Factor in Forming Surface Electric Field Basin in RESURF Lateral Power Devices and its Optimization Design. IEEE Journal of the Electron Devices Society, 2018, 6, 1147-1153.	1.2	5
128	Rethinking Sparsity in Performance Modeling for Analog and Mixed Circuits using Spike and Slab Models. , 2019, , .		5
129	TimingCamouflage+: Netlist Security Enhancement With Unconventional Timing. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 4482-4495.	1.9	5
130	Delving into Macro Placement with Reinforcement Learning. , 2021, , .		5
131	DREAMPlaceFPGA: An Open-Source Analytical Placer for Large Scale Heterogeneous FPGAs using Deep-Learning Toolkit. , 2022, , .		5
132	A novel intensity based optical proximity correction algorithm with speedup in lithography simulation. IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, 2007, , .	0.0	4
133	A Voltage-Frequency Island aware energy optimization framework for networks-on-chip. , 2008, , .		4
134	Voltage and frequency island optimizations for many-core/networks-on-chip designs. , 2010, , .		4
135	Incremental Layer Assignment Driven by an External Signoff Timing Engine. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 1126-1139.	1.9	4
136	Sequential Logic and Pipelining in Chip-Based Electronic-Photonic Digital Computing. IEEE Photonics Journal, 2020, 12, 1-11.	1.0	4
137	An Efficient Automatic Structure Design Method of Silicon-on-Insulator Lateral Power Device Considering RESURF Constraint. IEEE Transactions on Electron Devices, 2021, 68, 4593-4597.	1.6	4
138	Machine Learning in Physical Verification, Mask Synthesis, and Physical Design. , 2019, , 95-115.		4
139	AutoCRAFT: Layout Automation for Custom Circuits in Advanced FinFET Technologies. , 2022, , .		4
140	Light in AI: Toward Efficient Neurocomputing With Optical Neural Networksâ€"A Tutorial. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 2581-2585.	2.2	4
141	Stress Aware Layout Optimization Leveraging Active Area Dependent Mobility Enhancement. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2010, 29, 1533-1545.	1.9	3
142	Redundant Local-Loop Insertion for Unidirectional Routing. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 1113-1125.	1.9	3
143	Virtual-Tile-Based Flip-Flop Alignment Methodology for Clock Network Power Optimization. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 1256-1268.	2.1	3
144	Reinforcement Learning for Electronic Design Automation: Case Studies and Perspectives: (Invited) Tj ETQq0 0 0 rgBT /Overlock 10 Tf 50		3

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145	DPlace2.0: A stable and efficient analytical placement based on diffusion. , 2008, , .		2
146	Fast Substrate Noise Aware Floorplanning for Mixed Signal SOC Designs. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2008, 16, 1713-1717.	2.1	2
147	CSL: Coordinated and scalable logic synthesis techniques for effective NBTI reduction. , 2015, , .		2
148	An Improved Domain Decomposition Method for Drop Impact Reliability Analysis of 3-D ICs. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2018, 8, 1788-1799.	1.4	2
149	FPGA-Accelerated Spreading for Global Placement. , 2019, , .		2
150	SoulNet: ultrafast optical source optimization utilizing generative neural networks for advanced lithography. Journal of Micro/ Nanolithography, MEMS, and MOEMS, 2019, 18, 1.	1.0	2
151	Integrated WDM-based Optical Comparator for High-speed Computing. , 2020, , .		2
152	Wavelength-division-multiplexing-based electronic-photonic network for high-speed computing (Conference Presentation). , 2020, , .		2
153	Re-examining VLSI manufacturing and yield through the lens of deep learning. , 2020, , .		2
154	A Broadband Spectrum Channelizer With PWM-LO-Based Sub-Band Gain Control. IEEE Journal of Solid-State Circuits, 2022, 57, 781-792.	3.5	2
155	SqueezeLight: A Multi-Operand Ring-Based Optical Neural Network With Cross-Layer Scalability. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2023, 42, 807-819.	1.9	2
156	TIP-OPC: a new topological invariant paradigm for pixel based optical proximity correction. IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, 2007, , .	0.0	1
157	An accurate semi-analytical framework for full-chip TSV-induced stress modeling. , 2013, , .		1
158	A shape-driven spreading algorithm using linear programming for global placement. , 2019, , .		1
159	Power and Accuracy Co-Optimization of an Optical Full Adder via Optimization Algorithms. , 2019, , .		1
160	Tutorial and Perspectives on MAGICAL: A Silicon-Proven Open-Source Analog IC Layout System. IEEE Transactions on Circuits and Systems II: Express Briefs, 2023, 70, 715-720.	2.2	1
161	ELight: Toward Efficient and Aging-Resilient Photonic In-Memory Neurocomputing. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2023, 42, 820-833.	1.9	1
162	Long-range chromosomal interactions increase and mark repressed gene expression during adipogenesis. Epigenetics, 2022, 17, 1849-1862.	1.3	1

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163	Interactive Analog Layout Editing With Instant Placement and Routing Legalization. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2023, 42, 698-711.	1.9	1
164	Synthetic Biology Design and Analysis: A Case Study of Frequency Entrained Biological Clock. , 2008, , .		0
165	Doppler: DPL-aware and OPC-friendly gridless detailed routing with mask density balancing. , 2011, , .		0
166	Chemical-Mechanical Polishing-Aware Application-Specific 3D NoC Design. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2013, 32, 940-951.	1.9	0
167	Cut Redistribution and Insertion for Advanced 1-D Layout Design via Network Flow Optimization. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 1613-1626.	2.1	0
168	Fully Integrated 20 Gbit/s Silicon Optical Computing Chip for 4-Bit Full Adders. , 2019, , .		0
169	Report on the 38th ACM/IEEE International Conference on Computer-Aided Design (ICCAD 2019). IEEE Design and Test, 2020, 37, 121-122.	1.1	0
170	Experimental Demonstration of a WDM-based Integrated Optical Decoder for Compact Optical Computing. , 2021, , .		0
171	An Efficient Training Framework for Reversible Neural Architectures. Lecture Notes in Computer Science, 2020, , 275-289.	1.0	0
172	Practical Split Manufacturing Optimization. , 2020, , 9-38.		0