Soontae Kim

List of Publications by Year
in descending order

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39 papers	367 citations	1039406 9 h-index	996533 15 g-index
40 all docs	40 docs citations	40 times ranked	240 citing authors

#	Article	IF	Citations
1	Floating-ECC: Dynamic Repositioning of Error Correcting Code Bits for Extending the Lifetime of STT-RAM Caches. IEEE Transactions on Computers, 2016, 65, 3661-3675.	2.4	45
2	Residue cache. , 2011, , .		30
3	Ternary cache: Three-valued MLC STT-RAM caches. , 2014, , .		26
4	Predictive routing for mobile sinks in wireless sensor networks: a milestone-based approach. Journal of Supercomputing, 2012, 62, 1519-1536.	2.4	20
5	Subpage-Aware Solid State Drive for Improving Lifetime and Performance. IEEE Transactions on Computers, 2018, 67, 1492-1505.	2.4	20
6	Interpage-Based Endurance-Enhancing Lower State Encoding for MLC and TLC Flash Memory Storages. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 2033-2045.	2.1	17
7	Macho: A failure model-oriented adaptive cache architecture to enable near-threshold voltage scaling. , 2013, , .		16
8	Exploiting Same Tag Bits to Improve the Reliability of the Cache Memories. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 254-265.	2.1	16
9	Resuscitating privacy-preserving mobile payment with customer in complete control. Personal and Ubiquitous Computing, 2012, 16, 643-654.	1.9	14
10	Filter Data Cache: An Energy-Efficient Small L0 Data Cache Architecture Driven byMiss Cost Reduction. IEEE Transactions on Computers, 2015, 64, 1927-1939.	2.4	14
11	Lizard: Energy-efficient hard fault detection, diagnosis and isolation in the ALU. , 2010, , .		13
12	On load latency in low-power caches. , 2003, , .		10
13	A Restore-Free Mode for MLC STT-RAM Caches. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 1465-1469.	2.1	10
14	ECC-United Cache: Maximizing Efficiency of Error Detection/Correction Codes in Associative Cache Memories. IEEE Transactions on Computers, 2021, 70, 640-654.	2.4	9
15	TEPS: Transient Error Protection Utilizing Sub-word Parallelism. , 2009, , .		8
16	Skinflint DRAM system: Minimizing DRAM chip writes for low power. , 2013, , .		8
17	A Low-Cost Mechanism Exploiting Narrow-Width Values for Tolerating Hard Faults in ALU. IEEE Transactions on Computers, 2015, 64, 2433-2446.	2.4	8
18	MH Cache. Transactions on Architecture and Code Optimization, 2019, 16, 1-26.	1.6	7

#	Article	IF	Citations
19	Leveraging intra-page update diversity for mitigating write amplification in SSDs. , 2020, , .		7
20	SALE: Smartly Allocating Low-Cost Many-Bit ECC for Mitigating Read and Write Errors in STT-RAM Caches. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 1357-1370.	2.1	6
21	CID: Co-Architecting Instruction Cache and Decompression System for Embedded Systems. IEEE Transactions on Computers, 2021, 70, 1132-1145.	2.4	6
22	RAMS: DRAM Rank-Aware Memory Scheduling for Energy Saving. IEEE Transactions on Computers, 2016, 65, 3210-3216.	2.4	5
23	TLB Index-Based Tagging for Reducing Data Cache and TLB Energy Consumption. IEEE Transactions on Computers, 2017, 66, 1200-1211.	2.4	5
24	ENCORE Compression: Exploiting Narrow-width Values for Quantized Deep Neural Networks. , 2022, , .		5
25	ADSR: Angle-Based Multi-hop Routing Strategy for Mobile Wireless Sensor Networks. , 2011, , .		4
26	Adopting TLB index-based tagging to data caches for tag energy reduction. , 2012, , .		4
27	AVICA: An Access-time Variation Insensitive L1 Cache Architecture. , 2013, , .		4
28	Write Buffer-Oriented Energy Reduction in the L1 Data Cache for Embedded Systems. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 871-883.	2.1	4
29	Update Frequency-Directed Subpage Management for Mitigating Garbage Collection and DRAM Overheads. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 2467-2480.	1.9	4
30	Ensuring cache reliability and energy scaling at near-threshold voltage with Macho. IEEE Transactions on Computers, 2014, , 1-1.	2.4	3
31	Designing a Resilient L1 Cache Architecture to Process Variation-Induced Access-Time Failures. IEEE Transactions on Computers, 2016, 65, 2999-3012.	2.4	3
32	Exploiting Inter-block Entropy to Enhance the Compressibility of Blocks with Diverse Data. , 2022, , .		3
33	Salvaging Runtime Bad Blocks by Skipping Bad Pages for Improving SSD Performance. , 2022, , .		2
34	Performance-controllable shared cache architecture for multi-core soft real-time systems. , 2013, , .		1
35	Freezing: Eliminating Unnecessary Drawing Computation for Low Power. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 56-61.	1.9	1
36	SimTag: Exploiting tag bits similarity to improve the reliability of the data caches. , 2010, , .		0

#	Article	IF	Citations
37	High definition video transmisision using Bluetooth over UWB. , 2010, , .		0
38	Low-cost control flow error protection by exploiting available redundancies in the pipeline. , 2012, , .		0
39	Fault buffers. Design Automation for Embedded Systems, 2013, 17, 411-438.	0.7	0