Stephan EggersglÃ¼Ã

List of Publications by Year
in descending order

35 papers	243 citations	2258059 3 h-index	2272923 4 g-index
35 all docs	35 docs citations	35 times ranked	120 citing authors

#	Article	IF	Citations
1	On Reduction of Deterministic Test Pattern Sets. , 2021, , .		9
2	Cluster-based Localization of IR-drop in Test Application considering Parasitic Elements. , 2019, , .		3
3	Machine Learning-based Prediction of Test Power. , 2019, , .		12
4	Towards Complete Fault Coverage by Test Point Insertion using Optimization-SAT Techniques. , 2019, , .		0
5	Towards Complete Fault Coverage by Test Point Insertion using Optimization-SAT Techniques. , 2019, , .		2
6	Approximation-aware testing for approximate circuits. , 2018, , .		24
7	Optimization of retargeting for IEEE 1149.1 TAP controllers with embedded compression. , 2017, , .		6
8	Identification of Efficient Clustering Techniques for Test Power Activity on the Layout. , 2017, , .		6
9	Reconfigurable TAP controllers with embedded compression for large test data volume. , 2017, , .		4
10	Machine learning based test pattern analysis for localizing critical power activity areas. , 2017, , .		9
11	Revealing properties of structural materials by combining regression-based algorithms and nano indentation measurements. , 2017, , .		6
12	On Optimization-Based ATPG and Its Application for Highly Compacted Test Sets. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, 35, 2104-2117.	2.7	16
13	SAT-based post-processing for regional capture power reduction in at-speed scan test generation. , 2016, , .		5
14	VecTHOR: Low-cost compression architecture for IEEE 1149-compliant TAP controllers. , 2016, , .		6
15	Formal Test Point Insertion for Region-based Low-Capture-Power Compact At-Speed Scan Test. , 2016, , .		7
16	Compact test set generation for test compression-based designs. , 2015, , .		1
17	Automated formal verification of X propagation with respect to testability issues. , 2014, , .		0
18	Dynamic X-filling for Peak Capture Power Reduction for Compact Test Sets. Journal of Electronic Testing: Theory and Applications (JETTA), 2014, 30, 557-567.	1.2	3

#	Article	IF	Citations
19	Recent advances in SAT-based ATPG: Non-standard fault models, multi constraints and optimization. , 2014, , .		8
20	An effective fault ordering heuristic for SAT-based dynamic test compaction techniques. IT - Information Technology, 2014, 56, 157-164.	0.9	0
21	Test digitaler Schaltkreise. , 2014, , .		0
22	PASSAT 2.0: A multi-functional SAT-based testing framework. , 2013, , .		5
23	Peak Capture Power Reduction for Compact Test Sets Using Opt-Justification-Fill. , 2013, , .		3
24	Improved SAT-based ATPG: More constraints, better compaction. , 2013, , .		29
25	Robust Timing-Aware Test Generation Using Pseudo-Boolean Optimization. , 2012, , .		16
26	High Quality Test Pattern Generation and Boolean Satisfiability. , 2012, , .		14
27	As-Robust-As-Possible test generation in the presence of small delay defects using pseudo-Boolean optimization. , 2011, , .		15
28	Robust algorithms for high quality Test Pattern Generation using Boolean Satisfiability. , 2010, , .		7
29	MONSOON: SAT-Based ATPG for Path Delay Faults Using Multiple-Valued Logics. Journal of Electronic Testing: Theory and Applications (JETTA), 2010, 26, 307-322.	1.2	14
30	Efficient test generation with maximal crosstalk-induced noise using unconstrained aggressor excitation. , 2010, , .		2
31	Improving CNF representations in SAT-based ATPG for industrial circuits using BDDs. , 2010, , .		6
32	SWORD: A SAT like Prover Using Word Level Information. International Federation for Information Processing, 2009, , 1-17.	0.4	3
33	Effiziente ErfÃ¼llbarkeitsalgorithmen fÃ¼r die Generierung von TestmusternEfficient Satisfiability Solving Algorithms for Test Pattern Generation. IT - Information Technology, 2009, 51, 102-111.	0.9	0
34	Structural heuristics for SAT-based ATPG. , 2009, , .		1
35	Timing Arc Based Logic Analysis for false noise reduction. , 2009, , .		1