

Giuseppe Scotti

List of Publications by Year in Descending Order

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The third column is the impact factor (IF) of the journal, and the fourth column is the number of citations of the article.

108 papers	915 citations	16 h-index	24 g-index
135 ext. papers	1,193 ext. citations	2.3 avg, IF	4.59 L-index

#	Paper	IF	Citations
108	A Lightweight FPGA compatible weak-PUF primitive based on XOR gates. <i>IEEE Transactions on Circuits and Systems II: Express Briefs</i> , 2022 , 1-1	3.5	1
107	A Biasing Approach to Design Ultra-Low-Power Standard-Cell-Based Analog Building Blocks for Nanometer SoCs. <i>IEEE Access</i> , 2022 , 10, 25892-25900	3.5	3
106	A Tree-Based Architecture for High-Performance Ultra-Low-Voltage Amplifiers. <i>Journal of Low Power Electronics and Applications</i> , 2022 , 12, 12	1.7	5
105	A 0.5 V Sub-Threshold CMOS Current-Controlled Ring Oscillator for IoT and Implantable Devices. <i>Journal of Low Power Electronics and Applications</i> , 2022 , 12, 16	1.7	1
104	80dB tuning range transimpedance amplifier exploiting the Switched-Resistor approach. <i>AEU - International Journal of Electronics and Communications</i> , 2022 , 149, 154196	2.8	0
103	A Standard-Cell-Based CMFB for Fully Synthesizable OTAs. <i>Journal of Low Power Electronics and Applications</i> , 2022 , 12, 27	1.7	4
102	A Novel Ultra-Compact FPGA-compatible TRNG Architecture exploiting Latched Ring Oscillators. <i>IEEE Transactions on Circuits and Systems II: Express Briefs</i> , 2021 , 1-1	3.5	1
101	A Novel Standard-Cell-Based Implementation of the Digital OTA Suitable for Automatic Place and Route. <i>Journal of Low Power Electronics and Applications</i> , 2021 , 11, 42	1.7	5
100	A 0.3 V, Rail-to-Rail, Ultralow-Power, Non-Tailed, Body-Driven, Sub-Threshold Amplifier. <i>Applied Sciences (Switzerland)</i> , 2021 , 11, 2528	2.6	13
99	Klessydra-T: Designing Vector Coprocessors for Multithreaded Edge-Computing Cores. <i>IEEE Micro</i> , 2021 , 41, 64-71	1.8	4
98	A 0.3 V Rail-to-Rail Ultra-Low-Power OTA with Improved Bandwidth and Slew Rate. <i>Journal of Low Power Electronics and Applications</i> , 2021 , 11, 19	1.7	12
97	A Very-Low-Voltage Frequency Divider in Folded MOS Current Mode Logic With Complementary n- and p-type Flip-Flops. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , 2021 , 29, 998-1008	2.6	1
96	SC-DDPL as a Countermeasure against Static Power Side-Channel Attacks. <i>Cryptography</i> , 2021 , 5, 16	1.9	
95	0.5-V Frequency Dividers in Folded MCML Exploiting Forward Body Bias: Analysis and Comparison. <i>Electronics (Switzerland)</i> , 2021 , 10, 1383	2.6	
94	. <i>IEEE Transactions on Circuits and Systems I: Regular Papers</i> , 2021 , 68, 680-691	3.9	2
93	A Novel OTA Architecture Exploiting Current Gain Stages to Boost Bandwidth and Slew-Rate. <i>Electronics (Switzerland)</i> , 2021 , 10, 1638	2.6	4
92	Distributed switched-resistor approach for high-Q biquad filters. <i>AEU - International Journal of Electronics and Communications</i> , 2021 , 138, 153894	2.8	2

91	A Novel Ultra-Compact FPGA PUF: The DD-PUF. <i>Cryptography</i> , 2021 , 5, 23	1.9	7
90	0.5 V CMOS Inverter-Based Transconductance Amplifier with Quiescent Current Control. <i>Journal of Low Power Electronics and Applications</i> , 2021 , 11, 37	1.7	5
89	A SiGe HBT 6th-Order 10 GHz Inductor-Less Anti-Aliasing Low-Pass Filter for High-Speed ATI Digitizers. <i>IEEE Transactions on Circuits and Systems I: Regular Papers</i> , 2021 , 1-14	3.9	1
88	A Detailed Model of the Switched-Resistor Technique. <i>IEEE Open Journal of Circuits and Systems</i> , 2021 , 2, 497-507	1.7	1
87	A Power Efficient Frequency Divider With 55 GHz Self-Oscillating Frequency in SiGe BiCMOS. <i>Electronics (Switzerland)</i> , 2020 , 9, 1968	2.6	3
86	An improved reversed miller compensation technique for three-stage CMOS OTAs with double pole-zero cancellation and almost single-pole frequency response. <i>International Journal of Circuit Theory and Applications</i> , 2020 , 48, 1990-2005	2	3
85	SC-DDPL: A Novel Standard-Cell Based Approach for Counteracting Power Analysis Attacks in the Presence of Unbalanced Routing. <i>IEEE Transactions on Circuits and Systems I: Regular Papers</i> , 2020 , 67, 2317-2330	3.9	10
84	Delay models and design guidelines for MCML gates with resistor or PMOS load. <i>Microelectronics Journal</i> , 2020 , 99, 104755	1.8	4
83	10-GHz Fully Differential Sallen-Key Lowpass Biquad Filters in 55nm SiGe BiCMOS Technology. <i>Electronics (Switzerland)</i> , 2020 , 9, 563	2.6	1
82	A Multi-Folded MCML for Ultra-Low-Voltage High-Performance in Deeply Scaled CMOS. <i>IEEE Transactions on Circuits and Systems I: Regular Papers</i> , 2020 , 67, 4696-4706	3.9	3
81	Low power switched-resistor band-pass filter for neural recording channels in 130nm CMOS. <i>Heliyon</i> , 2020 , 6, e04723	3.6	4
80	0.6-V CMOS cascode OTA with complementary gate-driven gain-boosting and forward body bias. <i>International Journal of Circuit Theory and Applications</i> , 2020 , 48, 15-27	2	12
79	A Novel 0.5 V MCML D-Flip-Flop Topology Exploiting Forward Body Bias Threshold Lowering. <i>IEEE Transactions on Circuits and Systems II: Express Briefs</i> , 2020 , 67, 560-564	3.5	8
78	Area-Efficient Low-Power Bandpass Gm-C Filter for Epileptic Seizure Detection in 130nm CMOS 2019 ,		2
77	Secure Double Rate Registers as an RTL Countermeasure Against Power Analysis Attacks. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , 2018 , 26, 1368-1376	2.6	16
76	A Novel Very Low Voltage Topology to implement MCML XOR Gates 2018 ,		2
75	TEL Logic Style as a Countermeasure Against Side-Channel Attacks: Secure Cells Library in 65nm CMOS and Experimental Results. <i>IEEE Transactions on Circuits and Systems I: Regular Papers</i> , 2018 , 1-11	3.9	8
74	A Novel 0.6V MCML D-Latch Topology exploiting Dynamic Body Bias Threshold Lowering 2018 ,		1

73	Low power DDA-based instrumentation amplifier for neural recording applications in 65 nm CMOS. <i>AEU - International Journal of Electronics and Communications</i> , 2018 , 92, 30-35	2.8	19
72	Univariate Power Analysis Attacks Exploiting Static Dissipation of Nanometer CMOS VLSI Circuits for Cryptographic Applications. <i>IEEE Transactions on Emerging Topics in Computing</i> , 2017 , 5, 329-339	4.1	14
71	Multivariate Analysis Exploiting Static Power on Nanoscale CMOS Circuits for Cryptographic Applications. <i>Lecture Notes in Computer Science</i> , 2017 , 79-94	0.9	4
70	A Novel Framework to Estimate the Path Delay Variability On the Back of an Envelope via the Fan-Out-of-4 Metric. <i>IEEE Transactions on Circuits and Systems I: Regular Papers</i> , 2017 , 64, 2073-2085	3.9	12
69	0.9-V Class-AB Miller OTA in 0.35- μm CMOS With Threshold-Lowered Non-Tailed Differential Pair. <i>IEEE Transactions on Circuits and Systems I: Regular Papers</i> , 2017 , 64, 1740-1747	3.9	31
68	. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , 2017 , 25, 3509-3520	2.6	17
67	Template attacks exploiting static power and application to CMOS lightweight crypto-hardware. <i>International Journal of Circuit Theory and Applications</i> , 2017 , 45, 229-241	2	11
66	Novel measurements setup for attacks exploiting static power using DC pico-ammeter 2017 ,		4
65	CMOS Non-tailed differential pair. <i>International Journal of Circuit Theory and Applications</i> , 2016 , 44, 1468-1477	4	
64	Implementation of the PRESENT-80 block cipher and analysis of its vulnerability to Side Channel Attacks Exploiting Static Power 2016 ,		10
63	Design and validation through a frequency-based metric of a new countermeasure to protect nanometer ICs from side-channel attacks. <i>Journal of Cryptographic Engineering</i> , 2015 , 5, 269-288	1.9	11
62	High-tuning-range CMOS band-pass IF Filter based on a low-Q cascaded biquad optimization technique. <i>International Journal of Circuit Theory and Applications</i> , 2015 , 43, 1615-1636	2	7
61	Leakage Power Analysis attacks against a bit slice implementation of the Serpent block cipher 2014 ,		7
60	88- μs A 1-MHz Stray-Insensitive CMOS Current-Mode Interface IC for Differential Capacitive Sensors. <i>IEEE Transactions on Circuits and Systems I: Regular Papers</i> , 2014 , 61, 1905-1916	3.9	29
59	Effectiveness of Leakage Power Analysis Attacks on DPA-Resistant Logic Styles Under Process Variations. <i>IEEE Transactions on Circuits and Systems I: Regular Papers</i> , 2014 , 61, 429-442	3.9	36
58	Adaptive frequency compensation for maximum and constant bandwidth feedback amplifiers. <i>International Journal of Circuit Theory and Applications</i> , 2013 , 41, 424-440	2	3
57	Process and terminations variations aware stability criteria for microwave amplifiers. <i>International Journal of RF and Microwave Computer-Aided Engineering</i> , 2013 , 23, 619-626	1.5	
56	Constant and maximum bandwidth feedback amplifier with adaptive frequency compensation 2012 ,		3

55	Autotuning technique for CMOS current mode capacitive sensor interfaces 2012 ,		1
54	Exploiting the Body of MOS Devices for High Performance Analog Design. <i>IEEE Circuits and Systems Magazine</i> , 2011 , 11, 8-23	3.2	29
53	2011 ,		7
52	Avoiding the Gain-Bandwidth Trade Off in Feedback Amplifiers. <i>IEEE Transactions on Circuits and Systems I: Regular Papers</i> , 2011 , 58, 2108-2113	3.9	15
51	2011 ,		2
50	Delay-Based Dual-Rail Precharge Logic. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , 2011 , 19, 1147-1153	2.6	24
49	Reply to "Comments on Avoiding the Gain-Bandwidth Trade Off in Feedback Amplifiers". <i>IEEE Transactions on Circuits and Systems I: Regular Papers</i> , 2011 , 58, 2117-2117	3.9	1
48	Leakage Power Analysis attacks: Effectiveness on DPA resistant logic styles under process variations 2011 ,		4
47	Leakage Power Analysis Attacks: A Novel Class of Attacks to Nanometer Cryptographic Circuits. <i>IEEE Transactions on Circuits and Systems I: Regular Papers</i> , 2010 , 57, 355-367	3.9	68
46	On Practical Second-Order Power Analysis Attacks for Block Ciphers. <i>Lecture Notes in Computer Science</i> , 2010 , 155-170	0.9	1
45	Power analysis of a chaos-based Random Number Generator for cryptographic security 2009 ,		9
44	0.9-V CMOS cascode amplifier with body-driven gain boosting. <i>International Journal of Circuit Theory and Applications</i> , 2009 , 37, 193-202	2	25
43	Extraction of CAD-compatible statistical nonlinear models of GaAs HEMT MMICs. <i>Microwave and Optical Technology Letters</i> , 2009 , 51, 2163-2166	1.2	
42	The VCG-CCII: a novel building block and its application to capacitance multiplication. <i>Analog Integrated Circuits and Signal Processing</i> , 2009 , 58, 55-59	1.2	38
41	A novel low-voltage low-power fully differential voltage and current gained CCII for floating impedance simulations. <i>Microelectronics Journal</i> , 2009 , 40, 20-25	1.8	34
40	Impact of Process Variations on LPA Attacks Effectiveness 2009 ,		3
39	Design Solutions for Sample-and-Hold Circuits in CMOS Nanometer Technologies. <i>IEEE Transactions on Circuits and Systems II: Express Briefs</i> , 2009 , 56, 459-463	3.5	24
38	Delay-based dual-rail pre-charge logic 2009 ,		1

37	Analysis and Implementation of a Minimum-Supply Body-Biased CMOS Differential Amplifier Cell. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , 2009 , 17, 172-180	2.6	18
36	Differential Capacitance Analysis. <i>Lecture Notes in Computer Science</i> , 2009 , 338-347	0.9	
35	Unity-Gain Amplifier With Theoretically Zero Gain Error. <i>IEEE Transactions on Instrumentation and Measurement</i> , 2008 , 57, 1431-1437	5.2	4
34	2008 ,		1
33	Enhancing power analysis attacks against cryptographic devices. <i>IET Circuits, Devices and Systems</i> , 2008 , 2, 298	1.1	7
32	The Universal Circuit Simulator: A Mixed-Signal Approach to n -Port Network and Impedance Synthesis. <i>IEEE Transactions on Circuits and Systems I: Regular Papers</i> , 2007 , 54, 2178-2183	3.9	9
31	CMOS High-CMRR Current Output Stages. <i>IEEE Transactions on Circuits and Systems Part 2: Express Briefs</i> , 2007 , 54, 745-749		10
30	Linearization Technique for Source-Degenerated CMOS Differential Transconductors. <i>IEEE Transactions on Circuits and Systems Part 2: Express Briefs</i> , 2007 , 54, 848-852		28
29	CMOS Miller OTA with Body-Biased Output Stage 2007 ,		2
28	2007 ,		12
27	Analysis of data dependence of leakage current in CMOS cryptographic hardware 2007 ,		16
26	Very Low Voltage CMOS Two-stage Amplifier 2007 ,		1
25	A High-Speed Low-Voltage Phase Detector for Clock Recovery From NRZ Data. <i>IEEE Transactions on Circuits and Systems Part 1: Regular Papers</i> , 2007 , 54, 1626-1635		6
24	Sub-1V CMOS OTA with Body-driven Gain Boosting 2007 ,		6
23	A Statistical Model of Logic Gates for Monte Carlo Simulation Including On-Chip Variations. <i>Lecture Notes in Computer Science</i> , 2007 , 516-525	0.9	2
22	Discussion and new proofs of the conditional stability criteria for multidevice microwave amplifiers. <i>IET Microwaves Antennas and Propagation</i> , 2006 , 153, 177		4
21	High-CMRR Current Amplifier Architecture and Its CMOS Implementation. <i>IEEE Transactions on Circuits and Systems Part 2: Express Briefs</i> , 2006 , 53, 1118-1122		11
20	Stability Criterion for Two-Port Network With Input and Output Terminations Varying in Elliptic Regions. <i>IEEE Transactions on Microwave Theory and Techniques</i> , 2006 , 54, 4049-4055	4.1	4

19	. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , 2005 , 13, 191-200	2.6	4
18	A novel yield optimization technique for digital CMOS circuits design by means of process parameters run-time estimation and body bias active control. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , 2005 , 13, 630-638	2.6	25
17	An active balun for high-CMRR IC design 2005 ,		2
16	MMIC yield optimisation by design centring and off-chip controllers. <i>IET Circuits, Devices and Systems</i> , 2005 , 152, 54		16
15	Necessary and sufficient conditions for the stability of microwave amplifiers with variable termination impedances. <i>IEEE Transactions on Microwave Theory and Techniques</i> , 2005 , 53, 2580-2586	4.1	7
14	A Novel Dual-Output CCII-Based Single-Ended to Differential Converter. <i>Analog Integrated Circuits and Signal Processing</i> , 2005 , 43, 87-90	1.2	4
13	Biasing technique via bulk terminal for minimum supply CMOS amplifiers. <i>Electronics Letters</i> , 2005 , 41, 779	1.1	20
12	Behavioral model of a noisy VCO for efficient time-domain simulation. <i>Microwave and Optical Technology Letters</i> , 2004 , 40, 352-355	1.2	1
11	Yield Optimization by Means of Process Parameters Estimation: Comparison Between ABB and ASV Techniques. <i>Lecture Notes in Computer Science</i> , 2004 , 119-128	0.9	
10	A new procedure for nonlinear statistical model extraction of GaAs FET-integrated circuits. <i>International Journal of RF and Microwave Computer-Aided Engineering</i> , 2003 , 13, 348-356	1.5	1
9	Design of stable microwave multidevice circuits with complex termination impedances. <i>International Journal of RF and Microwave Computer-Aided Engineering</i> , 2002 , 12, 360-366	1.5	1
8	A bandwidth-compensated transimpedance amplifier for multigigabit optical receivers. <i>Microwave and Optical Technology Letters</i> , 2001 , 30, 79-81	1.2	0
7	Bias correction and yield optimization of MMICs with external digital control. <i>Microwave and Optical Technology Letters</i> , 2001 , 31, 134-137	1.2	1
6	Yield optimization design procedure of MMIC transimpedance amplifiers for multigigabit optical receivers. <i>Microwave and Optical Technology Letters</i> , 2000 , 26, 110-114	1.2	
5	A synthesis-oriented approach to design microwave multidevice amplifiers with a prefixed stability margin 2000 , 10, 102-104		7
4	A synthesis-oriented conditional stability criterion for microwave multidevice circuits with complex termination impedances 2000 , 10, 460-462		2
3	A synthesis-oriented approach to design stable circuits. <i>Microwave and Optical Technology Letters</i> , 1999 , 23, 354-357	1.2	6
2	A novel CMOS logic style with data independent power consumption		8

1 CMOS single-to-differential current amplifier

2