# Giuseppe Scotti

## List of Publications by Citations



| | | | |
|---|---|---|---|
| 108 papers | 915 citations | 16 h-index | 24 g-index |
| 135 ext. papers | 1,193 ext. citations | 2.3 avg, IF | 4.59 L-index |

| # | Paper | IF | Citations |
|---|---|---|---|
| 108 | Leakage Power Analysis Attacks: A Novel Class of Attacks to Nanometer Cryptographic Circuits. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2010**, 57, 355-367 | 3.9 | 68 |
| 107 | The VCG-CCII: a novel building block and its application to capacitance multiplication. *Analog Integrated Circuits and Signal Processing*, **2009**, 58, 55-59 | 1.2 | 38 |
| 106 | Effectiveness of Leakage Power Analysis Attacks on DPA-Resistant Logic Styles Under Process Variations. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2014**, 61, 429-442 | 3.9 | 36 |
| 105 | A novel low-voltage low-power fully differential voltage and current gained CCII for floating impedance simulations. *Microelectronics Journal*, **2009**, 40, 20-25 | 1.8 | 34 |
| 104 | 0.9-V Class-AB Miller OTA in 0.35- $mu text{m}$ CMOS With Threshold-Lowered Non-Tailed Differential Pair. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2017**, 64, 1740-1747 | 3.9 | 31 |
| 103 | 88-$mu$ A 1-MHz Stray-Insensitive CMOS Current-Mode Interface IC for Differential Capacitive Sensors. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2014**, 61, 1905-1916 | 3.9 | 29 |
| 102 | Exploiting the Body of MOS Devices for High Performance Analog Design. *IEEE Circuits and Systems Magazine*, **2011**, 11, 8-23 | 3.2 | 29 |
| 101 | Linearization Technique for Source-Degenerated CMOS Differential Transconductors. *IEEE Transactions on Circuits and Systems Part 2: Express Briefs*, **2007**, 54, 848-852 | | 28 |
| 100 | 0.9-V CMOS cascode amplifier with body-driven gain boosting. *International Journal of Circuit Theory and Applications*, **2009**, 37, 193-202 | 2 | 25 |
| 99 | A novel yield optimization technique for digital CMOS circuits design by means of process parameters run-time estimation and body bias active control. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2005**, 13, 630-638 | 2.6 | 25 |
| 98 | Delay-Based Dual-Rail Precharge Logic. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2011**, 19, 1147-1153 | 2.6 | 24 |
| 97 | Design Solutions for Sample-and-Hold Circuits in CMOS Nanometer Technologies. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2009**, 56, 459-463 | 3.5 | 24 |
| 96 | Biasing technique via bulk terminal for minimum supply CMOS amplifiers. *Electronics Letters*, **2005**, 41, 779 | 1.1 | 20 |
| 95 | Low power DDA-based instrumentation amplifier for neural recording applications in 65 nm CMOS. *AEU - International Journal of Electronics and Communications*, **2018**, 92, 30-35 | 2.8 | 19 |
| 94 | Analysis and Implementation of a Minimum-Supply Body-Biased CMOS Differential Amplifier Cell. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2009**, 17, 172-180 | 2.6 | 18 |
| 93 | . *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2017**, 25, 3509-3520 | 2.6 | 17 |
| 92 | Secure Double Rate Registers as an RTL Countermeasure Against Power Analysis Attacks. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2018**, 26, 1368-1376 | 2.6 | 16 |

| | | | |
|---|---|---|---|
| 91 | Analysis of data dependence of leakage current in CMOS cryptographic hardware **2007**, | | 16 |
| 90 | MMIC yield optimisation by design centring and off-chip controllers. *IET Circuits, Devices and Systems*, **2005**, 152, 54 | | 16 |
| 89 | Avoiding the Gain-Bandwidth Trade Off in Feedback Amplifiers. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2011**, 58, 2108-2113 | 3.9 | 15 |
| 88 | Univariate Power Analysis Attacks Exploiting Static Dissipation of Nanometer CMOS VLSI Circuits for Cryptographic Applications. *IEEE Transactions on Emerging Topics in Computing*, **2017**, 5, 329-339 | 4.1 | 14 |
| 87 | A 0.3 V, Rail-to-Rail, Ultralow-Power, Non-Tailed, Body-Driven, Sub-Threshold Amplifier. *Applied Sciences (Switzerland)*, **2021**, 11, 2528 | 2.6 | 13 |
| 86 | A Novel Framework to Estimate the Path Delay Variability On the Back of an Envelope via the Fan-Out-of-4 Metric. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2017**, 64, 2073-2085 | 3.9 | 12 |
| 85 | **2007**, | | 12 |
| 84 | A 0.3 V Rail-to-Rail Ultra-Low-Power OTA with Improved Bandwidth and Slew Rate. *Journal of Low Power Electronics and Applications*, **2021**, 11, 19 | 1.7 | 12 |
| 83 | 0.6-V CMOS cascode OTA with complementary gate-driven gain-boosting and forward body bias. *International Journal of Circuit Theory and Applications*, **2020**, 48, 15-27 | 2 | 12 |
| 82 | Design and validation through a frequency-based metric of a new countermeasure to protect nanometer ICs from side-channel attacks. *Journal of Cryptographic Engineering*, **2015**, 5, 269-288 | 1.9 | 11 |
| 81 | Template attacks exploiting static power and application to CMOS lightweight crypto-hardware. *International Journal of Circuit Theory and Applications*, **2017**, 45, 229-241 | 2 | 11 |
| 80 | High-CMRR Current Amplifier Architecture and Its CMOS Implementation. *IEEE Transactions on Circuits and Systems Part 2: Express Briefs*, **2006**, 53, 1118-1122 | | 11 |
| 79 | SC-DDPL: A Novel Standard-Cell Based Approach for Counteracting Power Analysis Attacks in the Presence of Unbalanced Routing. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2020**, 67, 2317-2330 | 3.9 | 10 |
| 78 | CMOS High-CMRR Current Output Stages. *IEEE Transactions on Circuits and Systems Part 2: Express Briefs*, **2007**, 54, 745-749 | | 10 |
| 77 | Implementation of the PRESENT-80 block cipher and analysis of its vulnerability to Side Channel Attacks Exploiting Static Power **2016**, | | 10 |
| 76 | Power analysis of a chaos-based Random Number Generator for cryptographic security **2009**, | | 9 |
| 75 | The Universal Circuit Simulator: A Mixed-Signal Approach to $n$-Port Network and Impedance Synthesis. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2007**, 54, 2178-2183 | 3.9 | 9 |
| 74 | TEL Logic Style as a Countermeasure Against Side-Channel Attacks: Secure Cells Library in 65nm CMOS and Experimental Results. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2018**, 1-11 | 3.9 | 8 |

| | | | |
|---|---|---|---|
| 73 | A novel CMOS logic style with data independent power consumption | | 8 |
| 72 | A Novel 0.5 V MCML D-Flip-Flop Topology Exploiting Forward Body Bias Threshold Lowering. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2020**, 67, 560-564 | 3.5 | 8 |
| 71 | High-tuning-range CMOS band-pass IF filter based on a low-Q cascaded biquad optimization technique. *International Journal of Circuit Theory and Applications*, **2015**, 43, 1615-1636 | 2 | 7 |
| 70 | Leakage Power Analysis attacks against a bit slice implementation of the Serpent block cipher **2014** , | | 7 |
| 69 | **2011**, | | 7 |
| 68 | Enhancing power analysis attacks against cryptographic devices. *IET Circuits, Devices and Systems*, **2008**, 2, 298 | 1.1 | 7 |
| 67 | Necessary and sufficient conditions for the stability of microwave amplifiers with variable termination impedances. *IEEE Transactions on Microwave Theory and Techniques*, **2005**, 53, 2580-2586 | 4.1 | 7 |
| 66 | A synthesis-oriented approach to design microwave multidevice amplifiers with a prefixed stability margin **2000**, 10, 102-104 | | 7 |
| 65 | A Novel Ultra-Compact FPGA PUF: The DD-PUF. *Cryptography*, **2021**, 5, 23 | 1.9 | 7 |
| 64 | A High-Speed Low-Voltage Phase Detector for Clock Recovery From NRZ Data. *IEEE Transactions on Circuits and Systems Part 1: Regular Papers*, **2007**, 54, 1626-1635 | | 6 |
| 63 | Sub-1V CMOS OTA with Body-driven Gain Boosting **2007**, | | 6 |
| 62 | A synthesis-oriented approach to design stable circuits. *Microwave and Optical Technology Letters*, **1999**, 23, 354-357 | 1.2 | 6 |
| 61 | A Novel Standard-Cell-Based Implementation of the Digital OTA Suitable for Automatic Place and Route. *Journal of Low Power Electronics and Applications*, **2021**, 11, 42 | 1.7 | 5 |
| 60 | 0.5 V CMOS Inverter-Based Transconductance Amplifier with Quiescent Current Control. *Journal of Low Power Electronics and Applications*, **2021**, 11, 37 | 1.7 | 5 |
| 59 | A Tree-Based Architecture for High-Performance Ultra-Low-Voltage Amplifiers. *Journal of Low Power Electronics and Applications*, **2022**, 12, 12 | 1.7 | 5 |
| 58 | Multivariate Analysis Exploiting Static Power on Nanoscale CMOS Circuits for Cryptographic Applications. *Lecture Notes in Computer Science*, **2017**, 79-94 | 0.9 | 4 |
| 57 | Delay models and design guidelines for MCML gates with resistor or PMOS load. *Microelectronics Journal*, **2020**, 99, 104755 | 1.8 | 4 |
| 56 | Novel measurements setup for attacks exploiting static power using DC pico-ammeter **2017**, | | 4 |

| | | | |
|---|---|---|---|
| 55 | Leakage Power Analysis attacks: Effectiveness on DPA resistant logic styles under process variations **2011**, | | 4 |
| 54 | Unity-Gain Amplifier With Theoretically Zero Gain Error. *IEEE Transactions on Instrumentation and Measurement*, **2008**, 57, 1431-1437 | 5.2 | 4 |
| 53 | Discussion and new proofs of the conditional stability criteria for multidevice microwave amplifiers. *IET Microwaves Antennas and Propagation*, **2006**, 153, 177 | | 4 |
| 52 | . *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2005**, 13, 191-200 | 2.6 | 4 |
| 51 | Stability Criterion for Two-Port Network With Input and Output Terminations Varying in Elliptic Regions. *IEEE Transactions on Microwave Theory and Techniques*, **2006**, 54, 4049-4055 | 4.1 | 4 |
| 50 | A Novel Dual-Output CCII-Based Single-Ended to Differential Converter. *Analog Integrated Circuits and Signal Processing*, **2005**, 43, 87-90 | 1.2 | 4 |
| 49 | Low power switched-resistor band-pass filter for neural recording channels in 130nm CMOS. *Heliyon*, **2020**, 6, e04723 | 3.6 | 4 |
| 48 | Klessydra-T: Designing Vector Coprocessors for Multithreaded Edge-Computing Cores. *IEEE Micro*, **2021**, 41, 64-71 | 1.8 | 4 |
| 47 | CMOS Non-tailed differential pair. *International Journal of Circuit Theory and Applications*, **2016**, 44, 1468-1477 | | 4 |
| 46 | A Novel OTA Architecture Exploiting Current Gain Stages to Boost Bandwidth and Slew-Rate. *Electronics (Switzerland)*, **2021**, 10, 1638 | 2.6 | 4 |
| 45 | A Standard-Cell-Based CMFB for Fully Synthesizable OTAs. *Journal of Low Power Electronics and Applications*, **2022**, 12, 27 | 1.7 | 4 |
| 44 | A Power Efficient Frequency Divider With 55 GHz Self-Oscillating Frequency in SiGe BiCMOS. *Electronics (Switzerland)*, **2020**, 9, 1968 | 2.6 | 3 |
| 43 | An improved reversed miller compensation technique for three-stage CMOS OTAs with double pole-zero cancellation and almost single-pole frequency response. *International Journal of Circuit Theory and Applications*, **2020**, 48, 1990-2005 | 2 | 3 |
| 42 | Adaptive frequency compensation for maximum and constant bandwidth feedback amplifiers. *International Journal of Circuit Theory and Applications*, **2013**, 41, 424-440 | 2 | 3 |
| 41 | Constant and maximum bandwidth feedback amplifier with adaptive frequency compensation **2012** , | | 3 |
| 40 | Impact of Process Variations on LPA Attacks Effectiveness **2009**, | | 3 |
| 39 | A Multi-Folded MCML for Ultra-Low-Voltage High-Performance in Deeply Scaled CMOS. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2020**, 67, 4696-4706 | 3.9 | 3 |
| 38 | A Biasing Approach to Design Ultra-Low-Power Standard-Cell-Based Analog Building Blocks for Nanometer SoCs. *IEEE Access*, **2022**, 10, 25892-25900 | 3.5 | 3 |

| | | | |
|---|---|---|---|
| 37 | A Novel Very Low Voltage Topology to implement MCML XOR Gates **2018**, | | 2 |
| 36 | **2011**, | | 2 |
| 35 | CMOS Miller OTA with Body-Biased Output Stage **2007**, | | 2 |
| 34 | An active balun for high-CMRR IC design **2005**, | | 2 |
| 33 | CMOS single-to-differential current amplifier | | 2 |
| 32 | A synthesis-oriented conditional stability criterion for microwave multidevice circuits with complex termination impedances **2000**, 10, 460-462 | | 2 |
| 31 | A Statistical Model of Logic Gates for Monte Carlo Simulation Including On-Chip Variations. *Lecture Notes in Computer Science*, **2007**, 516-525 | 0.9 | 2 |
| 30 | Area-Efficient Low-Power Bandpass Gm-C Filter for Epileptic Seizure Detection in 130nm CMOS **2019**, | | 2 |
| 29 | . *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2021**, 68, 680-691 | 3.9 | 2 |
| 28 | Distributed switched-resistor approach for high-Q biquad filters. *AEU - International Journal of Electronics and Communications*, **2021**, 138, 153894 | 2.8 | 2 |
| 27 | 10-GHz Fully Differential Sallen-Key Lowpass Biquad Filters in 55nm SiGe BiCMOS Technology. *Electronics (Switzerland)*, **2020**, 9, 563 | 2.6 | 1 |
| 26 | Reply to "Comments on Avoiding the Gain-Bandwidth Trade Off in Feedback Amplifiers". *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2011**, 58, 2117-2117 | 3.9 | 1 |
| 25 | Autotuning technique for CMOS current mode capacitive sensor interfaces **2012**, | | 1 |
| 24 | Delay-based dual-rail pre-charge logic **2009**, | | 1 |
| 23 | **2008**, | | 1 |
| 22 | Very Low Voltage CMOS Two-stage Amplifier **2007**, | | 1 |
| 21 | Behavioral model of a noisy VCO for efficient time-domain simulation. *Microwave and Optical Technology Letters*, **2004**, 40, 352-355 | 1.2 | 1 |
| 20 | Design of stable microwave multidevice circuits with complex termination impedances. *International Journal of RF and Microwave Computer-Aided Engineering*, **2002**, 12, 360-366 | 1.5 | 1 |

| | | | |
|---|---|---|---|
| 19 | A new procedure for nonlinear statistical model extraction of GaAs FET-integrated circuits. *International Journal of RF and Microwave Computer-Aided Engineering*, **2003**, 13, 348-356 | 1.5 | 1 |
| 18 | Bias correction and yield optimization of MMICs with external digital control. *Microwave and Optical Technology Letters*, **2001**, 31, 134-137 | 1.2 | 1 |
| 17 | A Novel Ultra-Compact FPGA-compatible TRNG Architecture exploiting Latched Ring Oscillators. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2021**, 1-1 | 3.5 | 1 |
| 16 | On Practical Second-Order Power Analysis Attacks for Block Ciphers. *Lecture Notes in Computer Science*, **2010**, 155-170 | 0.9 | 1 |
| 15 | A Very-Low-Voltage Frequency Divider in Folded MOS Current Mode Logic With Complementary n- and p-type Flip-Flops. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2021**, 29, 998-1008 | 2.6 | 1 |
| 14 | A Novel 0.6V MCML D-Latch Topology exploiting Dynamic Body Bias Threshold Lowering **2018**, | | 1 |
| 13 | A SiGe HBT 6th-Order 10 GHz Inductor-Less Anti-Aliasing Low-Pass Filter for High-Speed ATI Digitizers. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2021**, 1-14 | 3.9 | 1 |
| 12 | A Detailed Model of the Switched-Resistor Technique. *IEEE Open Journal of Circuits and Systems*, **2021**, 2, 497-507 | 1.7 | 1 |
| 11 | A Lightweight FPGA compatible weak-PUF primitive based on XOR gates. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2022**, 1-1 | 3.5 | 1 |
| 10 | A 0.5 V Sub-Threshold CMOS Current-Controlled Ring Oscillator for IoT and Implantable Devices. *Journal of Low Power Electronics and Applications*, **2022**, 12, 16 | 1.7 | 1 |
| 9 | A bandwidth-compensated transimpedance amplifier for multigigabit optical receivers. *Microwave and Optical Technology Letters*, **2001**, 30, 79-81 | 1.2 | 0 |
| 8 | 80 dB tuning range transimpedance amplifier exploiting the Switched-Resistor approach. *AEU - International Journal of Electronics and Communications*, **2022**, 149, 154196 | 2.8 | 0 |
| 7 | Process and terminations variations aware stability criteria for microwave amplifiers. *International Journal of RF and Microwave Computer-Aided Engineering*, **2013**, 23, 619-626 | 1.5 | |
| 6 | Extraction of CAD-compatible statistical nonlinear models of GaAs HEMT MMICs. *Microwave and Optical Technology Letters*, **2009**, 51, 2163-2166 | 1.2 | |
| 5 | Yield optimization design procedure of MMIC transimpedance amplifiers for multigigabit optical receivers. *Microwave and Optical Technology Letters*, **2000**, 26, 110-114 | 1.2 | |
| 4 | Yield Optimization by Means of Process Parameters Estimation: Comparison Between ABB and ASV Techniques. *Lecture Notes in Computer Science*, **2004**, 119-128 | 0.9 | |
| 3 | Differential Capacitance Analysis. *Lecture Notes in Computer Science*, **2009**, 338-347 | 0.9 | |
| 2 | SC-DDPL as a Countermeasure against Static Power Side-Channel Attacks. *Cryptography*, **2021**, 5, 16 | 1.9 | |

1 0.5-V Frequency Dividers in Folded MCML Exploiting Forward Body Bias: Analysis and Comparison. *Electronics (Switzerland)*, **2021**, 10, 1383 2.6