Meysam Zareiee

List of Publications by Year
in descending order

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16	205	933447	1281871
papers	citations	10	11
		h-index	g-index

17	17	17	100
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	A new architecture of the dual gate transistor for the analog and digital applications. AEU - International Journal of Electronics and Communications, 2019, 100, 114-118.	2.9	15
2	A New Structure for Lateral Double Diffused MOSFET to Control the Breakdown Voltage and the On-Resistance. Silicon, 2019, 11, 3011-3019.	3.3	14
3	A novel dual trench gate power device by effective drift region structure. Superlattices and Microstructures, 2019, 125, 8-15.	3.1	9
4	Inserting PN junction in a power device for achieving improved figure of merit. , 2018, , .		3
5	High Performance Nano Device with Reduced Short Channel Effects in High Temperature Applications. ECS Journal of Solid State Science and Technology, 2017, 6, M75-M78.	1.8	17
6	Superior electrical characteristics of novel nanoscale MOSFET with embedded tunnel diode. Superlattices and Microstructures, 2017, 101, 57-67.	3.1	13
7	A Reliable Nano Device with Appropriate Performance in High Temperatures. ECS Journal of Solid State Science and Technology, 2017, 6, M50-M54.	1.8	12
8	Controlled Kink Effect in a Novel High-Voltage LDMOS Transistor by Creating Local Minimum in Energy Band Diagram. IEEE Transactions on Electron Devices, 2017, 64, 4213-4218.	3.0	29
9	A reliable high performance nano SOI MOSFET by considering quadruple silicon zones. , 2017, , .		0
10	Modifying Buried Layers in Nano-MOSFET for Achieving Reliable Electrical Characteristics. ECS Journal of Solid State Science and Technology, 2016, 5, M113-M117.	1.8	12
11	Improved Device Performance in Nano Scale Transistor: An Extended Drain SOI MOSFET. ECS Journal of Solid State Science and Technology, 2016, 5, M74-M77.	1.8	26
12	A novel high breakdown voltage LDMOS by protruded silicon dioxide at the drift region. Journal of Computational Electronics, 2016, 15, 611-618.	2.5	29
13	A novel high performance nano-scale MOSFET by inserting Si3N4 layer in the channel. Superlattices and Microstructures, 2015, 88, 254-261.	3.1	23
14	Î-Shape Silicon Window for Controlling OFF-Current in Junctionless SOI MOSFET. Silicon, 0, , 1.	3.3	0
15	Using Hetro-Structure Window in Nano Scale Junctionless SOI MOSFET for High Electrical Performance. ECS Journal of Solid State Science and Technology, 0, , .	1.8	2
16	SiC Material in Si-LDMOS Transistors by Controlling Mismatching at Their Interfaces. Journal of Electronic Materials, 0, , .	2.2	1