

# Yongliang Li

## List of Publications by Year in descending order

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50  
papers

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citations

1040056

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1125743

13  
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docs citations

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times ranked

154  
citing authors

#	ARTICLE	IF	CITATIONS
1	Si <sub>0.5</sub> Ge <sub>0.5</sub> channel introduction technique for the preparation of high mobility FinFET device. Materials Science in Semiconductor Processing, 2022, 139, 106373.	4.0	2
2	A Polarization-Switching, Charge-Trapping, Modulated Arithmetic Logic Unit for In-Memory Computing Based on Ferroelectric Fin Field-Effect Transistors. ACS Applied Materials & Interfaces, 2022, 14, 6967-6976.	8.0	10
3	Improving Driving Current with High-Efficiency Landing Pads Technique for Reduced Parasitic Resistance in Gate-All-Around Si Nanosheet Devices. ECS Journal of Solid State Science and Technology, 2022, 11, 035010.	1.8	4
4	4-Levels Vertically Stacked SiGe Channel Nanowires Gate-All-Around Transistor with Novel Channel Releasing and Source and Drain Silicide Process. Nanomaterials, 2022, 12, 889.	4.1	7
5	Low-Temperature (â%500 Å°C) Complementary Schottky Source/Drain FinFETs for 3D Sequential Integration. Nanomaterials, 2022, 12, 1218.	4.1	0
6	Insertion of Hafnium Interlayer to Improve the Thermal Stability of Ultrathin TiSi <sub>x</sub> in TiSi <sub>x</sub> /n <sup>+</sup> -Si Ohmic Contacts. IEEE Transactions on Electron Devices, 2022, 69, 3347-3352.	3.0	3
7	Ultralow Contact Resistivity on Ga-Doped Ge with Contact Co-Implantation of Ge and B. ECS Journal of Solid State Science and Technology, 2022, 11, 054002.	1.8	1
8	Fabrication and selective wet etching of Si <sub>0.2</sub> Ge <sub>0.8</sub> /Ge multilayer for Si <sub>0.2</sub> Ge <sub>0.8</sub> channel gate-all-around MOSFETs. Materials Science in Semiconductor Processing, 2021, 121, 105397.	4.0	8
9	Optimization of zero-level interlayer dielectric materials for gate-all-around silicon nanowire channel fabrication in a replacement metal gate process. Materials Science in Semiconductor Processing, 2021, 121, 105434.	4.0	5
10	Experimental Investigation of As Preamorphization Implant on Electrical Property of Ti-Based Silicide Contacts. IEEE Transactions on Electron Devices, 2021, 68, 1835-1840.	3.0	5
11	Investigate on the Mechanism of HfO <sub>2</sub> /Si <sub>0.7</sub> Ge <sub>0.3</sub> Interface Passivation Based on Low-Temperature Ozone Oxidation and Si-Cap Methods. Nanomaterials, 2021, 11, 955.	4.1	7
12	Four-Period Vertically Stacked SiGe/Si Channel FinFET Fabrication and Its Electrical Characteristics. Nanomaterials, 2021, 11, 1689.	4.1	10
13	Vertical Sandwich GAA FETs With Self-Aligned High-κ Metal Gate Made by Quasi Atomic Layer Etching Process. IEEE Transactions on Electron Devices, 2021, 68, 2604-2610.	3.0	21
14	Novel Si/SiGe fin on insulator fabrication on bulk-Si substrate. Materials Research Express, 2021, 8, 075902.	1.6	1
15	Fabrication of High-Mobility Si <sub>0.7</sub> Ge <sub>0.3</sub> Channel FinFET for Optimization of Device Electrical Performance. ECS Journal of Solid State Science and Technology, 2021, 10, 075001.	1.8	3
16	Thermal stability issue of ultrathin Ti-based silicide for its application in prospective DRAM peripheral 3D FinFET transistors. Journal of Materials Science: Materials in Electronics, 2021, 32, 24107-24114.	2.2	4
17	Investigation of thermal stability of Si <sub>0.7</sub> Ge <sub>0.3</sub> Si stacked multilayer with As ion-implantation. Materials Research Express, 2021, 8, 095007.	1.6	0
18	A Novel Method to Reduce Specific Contact Resistivity of TiSi <sub>x</sub> /n <sup>+</sup> -Si Contacts by Employing an In-Situ Steam Generation Oxidation Prior to Ti Silicidation. IEEE Electron Device Letters, 2021, 42, 958-961.	3.9	4

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19	Integration of Si <sub>0.7</sub> Ge <sub>0.3</sub> fin onto a bulk-Si substrate and its P-type FinFET device fabrication. Semiconductor Science and Technology, 2021, 36, 125001.	2.0	3
20	Comparison of DC/AC Hot Carrier Degradation between Short Channel Si Bulk and SiGe SOI p-FinFETs. , 2021, , .		0
21	Study of selective isotropic etching Si <sub>1-x</sub> Ge <sub>x</sub> in process of nanowire transistors. Journal of Materials Science: Materials in Electronics, 2020, 31, 134-143.	2.2	14
22	Investigation on the formation technique of SiGe Fin for the high mobility channel FinFET device. Journal of Materials Science: Materials in Electronics, 2020, 31, 5854-5860.	2.2	2
23	Experimental study of the ultrathin oxides on SiGe alloy formed by low-temperature ozone oxidation. Materials Science in Semiconductor Processing, 2020, 107, 104832.	4.0	7
24	Selective wet etching in fabricating SiGe nanowires with TMAH solution for gate-all-around MOSFETs. Journal of Materials Science: Materials in Electronics, 2020, 31, 22478-22486.	2.2	7
25	Impact of Charges at Ferroelectric/Interlayer Interface on Depolarization Field of Ferroelectric FET With Metal/Ferroelectric/Interlayer/Si Gate-Stack. IEEE Transactions on Electron Devices, 2020, 67, 4500-4506.	3.0	20
26	Investigation of Ultrathin Ni Germanosilicide for Advanced pMOS Contact Metallization. IEEE Transactions on Electron Devices, 2020, 67, 5039-5044.	3.0	2
27	Understanding Frequency Dependence of Trap Generation Under AC Negative Bias Temperature Instability Stress in Si p-FinFETs. IEEE Electron Device Letters, 2020, 41, 965-968.	3.9	11
28	Insights Into the Effect of TiN Thickness Scaling on DC and AC NBTI Characteristics in Replacement Metal Gate pMOSFETs. IEEE Transactions on Device and Materials Reliability, 2020, 20, 498-505.	2.0	3
29	Role of Carbon Pre-Germanidation Implantation on Enhancing the Thermal Stability of NiGe Films Below 10 nm Thickness. ECS Journal of Solid State Science and Technology, 2020, 9, 054006.	1.8	4
30	A Novel Dry Selective Isotropic Atomic Layer Etching of SiGe for Manufacturing Vertical Nanowire Array with Diameter Less than 20 nm. Materials, 2020, 13, 771.	2.9	8
31	Understanding the mechanisms impacting the interface states of ozone-treated high-k/SiGe interfaces. Semiconductor Science and Technology, 2020, 35, 055018.	2.0	3
32	Fabrication technique of the Si <sub>0.5</sub> Ge <sub>0.5</sub> Fin for the high mobility channel FinFET device. Semiconductor Science and Technology, 2020, 35, 045015.	2.0	12
33	An Investigation of Field Reduction Effect on NBTI Parameter Characterization and Lifetime Prediction Using a Constant Field Stress Method. IEEE Transactions on Device and Materials Reliability, 2020, 20, 92-96.	2.0	3
34	Comparative study on NBTI kinetics in Si p-FinFETs with B <sub>2</sub> H <sub>6</sub> -based and SiH <sub>4</sub> -based atomic layer deposition tungsten (ALD W) filling metal. Microelectronics Reliability, 2020, 107, 113627.	1.7	5
35	Study of Silicon Nitride Inner Spacer Formation in Process of Gate-all-around Nano-Transistors. Nanomaterials, 2020, 10, 793.	4.1	19
36	Investigation of Barrier Property of Amorphous Co/Ti Layer as Single Barrier/Liner in Local Co Interconnects. IEEE Transactions on Electron Devices, 2020, 67, 2076-2081.	3.0	7

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37	Investigation on thermal stability of Si <sub>0.7</sub> Ge <sub>0.3</sub> /Si stacked multilayer for gate-all-around MOSFETS. Semiconductor Science and Technology, 2020, 35, 115008.	2.0	10
38	Key Process Technologies for Stacked Double Si <sub>0.7</sub> Ge <sub>0.3</sub> Channel Nanowires Fabrication. ECS Journal of Solid State Science and Technology, 2020, 9, 064009.	1.8	6
39	Identification of a suitable passivation route for high-k/SiGe interface based on ozone oxidation. Applied Surface Science, 2019, 493, 478-484.	6.1	8
40	A novel three-layer graded SiGe strain relaxed buffer for the high crystal quality and strained Si <sub>0.5</sub> Ge <sub>0.5</sub> layer epitaxial grown. Journal of Materials Science: Materials in Electronics, 2019, 30, 14130-14135.	2.2	6
41	Process optimization of the Si <sub>0.7</sub> Ge <sub>0.3</sub> Fin Formation for the STI first scheme. Semiconductor Science and Technology, 2019, 34, 125008.	2.0	10
42	Comprehensive Study and Design of High-k/SiGe Gate Stacks with Interface-Engineering by Ozone Oxidation. ECS Journal of Solid State Science and Technology, 2019, 8, N100-N105.	1.8	5
43	Investigation of NiGe Films Formed on Both n <sup>+</sup> - and p <sup>+</sup> -Ge with P and B Ion Implantation before Germanidation. ECS Journal of Solid State Science and Technology, 2019, 8, P271-P276.	1.8	0
44	High crystal quality strained Si <sub>0.5</sub> Ge <sub>0.5</sub> layer with a thickness of up to 50 nm grown on the three-layer SiGe strain relaxed buffer. Materials Science in Semiconductor Processing, 2019, 99, 159-164.	4.0	8
45	Fabrication Technique for pMOSFET poly-Si/TaN/TiN/HfSiAlON Gate Stack. ECS Journal of Solid State Science and Technology, 2018, 7, P537-P540.	1.8	0
46	Physical Mechanism Underlying the Time Exponent Shift in the Ultra-fast NBTI of High-k/Metal gated p-CMOSFETs. , 2018, , .		8
47	Dry Etching of Metal Inserted Poly-Si Stack for Dual High-k and Dual Metal Gate Integration. ECS Journal of Solid State Science and Technology, 2018, 7, P435-P439.	1.8	0
48	Investigation of Key Technologies for Poly-Si/TaN/HfLaON/IL $\text{SiO}_2$ Gate-Stacks in Advanced Device Applications. IEEE Transactions on Electron Devices, 2014, 61, 991-997.	3.0	1
49	The fabrication and dry etching of poly-Si/TaN/Mo gate stack in the metal inserted poly-Si stack structure. Microelectronic Engineering, 2011, 88, 976-980.	2.4	4
50	Dry etching of poly-Si/TaN/HfSiON gate stack for advanced complementary metal-oxide-semiconductor devices. Journal of Semiconductors, 2011, 32, 076001.	3.7	2