Tetsuo Endoh

List of Publications by Year
in descending order

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80 papers	1,045 citations	687363 13 h-index	526287 27 g-index
80 all docs	80 docs citations	80 times ranked	786 citing authors

#	Article	IF	Citations
1	Efficient BCH Code Encoding and Decoding Algorithm With Divisor-Distance-Based Polynomial Division for STT-MRAM. IEEE Transactions on Magnetics, 2023, 59, 1-8.	2.1	1
2	Energy-Efficient Convolution Module With Flexible Bit-Adjustment Method and ADC Multiplier Architecture for Industrial IoT. IEEE Transactions on Industrial Informatics, 2022, 18, 3055-3065.	11.3	3
3	Perpendicular Magnetic Tunnel Junctions With Four Anti-Ferromagnetically Coupled Co/Pt Pinning Layers. IEEE Transactions on Magnetics, 2022, 58, 1-5.	2.1	3
4	Effect of Magnetic Coupling Between Two CoFeB Layers on Thermal Stability in Perpendicular Magnetic Tunnel Junctions With MgO/CoFeB/Insertion Layer/CoFeB/MgO Free Layer. IEEE Transactions on Magnetics, 2022, 58, 1-6.	2.1	2
5	Influence of Iridium Sputtering Conditions on the Magnetic Properties of Co/Pt-Based Iridium-Synthetic Antiferromagnetic Coupling Reference Layer. IEEE Transactions on Magnetics, 2022, 58, 1-5.	2.1	1
6	Enhancement of current to spin-current conversion and spin torque efficiencies in a synthetic antiferromagnetic layer based on a Pt/Ir/Pt spacer layer. Physical Review B, 2022, 105, .	3.2	11
7	Structural Analysis of CoFeB/MgO-Based Perpendicular MTJs With Junction Size of 20 nm by STEM Tomography. IEEE Transactions on Magnetics, 2021, 57, 1-7.	2.1	0
8	40 nm 1Tâ€“1MTJ 128 Mb STT-MRAM With Novel Averaged Reference Voltage Generator Based on Detailed Analysis of Scaled-Down Memory Cell Array Design. IEEE Transactions on Magnetics, 2021, 57, 1-9.	2.1	3
9	Dual-Port SOT-MRAM Achieving 90-MHz Read and 60-MHz Write Operations Under Field-Assistance-Free Condition. IEEE Journal of Solid-State Circuits, 2021, 56, 1116-1128.	5.4	24
10	Highly accurate and efficient cluster validation index engine using global separation and local dispersion architecture for adaptive image clustering systems. Japanese Journal of Applied Physics, 2021, 60, SBBL02.	1.5	0
11	Enhancement of magnetic coupling and magnetic anisotropy in MTJs with multiple CoFeB/MgO interfaces for high thermal stability. AIP Advances, 2021, 11, .	1.3	6
12	Oxidation of Silicon Nanopillars. Journal of Physical Chemistry C, 2021, 125, 8853-8861.	3.1	4
13	State-of-the-Art Power Devices and Power Electronics Integration Technology. Journal of Japan Institute of Electronics Packaging, 2021, 24, 215-225.	0.1	1
14	First Demonstration of 25-nm Quad Interface p-MTJ Device With Low Resistance-Area Product MgO and Ten Years Retention for High Reliable STT-MRAM. IEEE Transactions on Electron Devices, 2021, 68, 2680-2685.	3.0	8
15	Precise fabrication of uniform sub-10-nm-diameter cylindrical silicon nanopillars via oxidation control. Scripta Materialia, 2021, 198, 113818.	5.2	8
16	Ultimate vertical gate-all-around metalâ€“oxideâ€“semiconductor field-effect transistor and its three-dimensional integrated circuits. Materials Science in Semiconductor Processing, 2021, 134, 106046.	4.0	15
17	Synthetic antiferromagnetic layer based on Pt/Ru/Pt spacer layer with 1.05â€‰nm interlayer exchange oscillation period for spinâ€“orbit torque devices. Applied Physics Letters, 2021, 119, .	3.3	11
18	Low-density oxide grown thermally on sidewall of Si nanopillars. Materials Letters, 2020, 258, 126780.	2.6	4

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19	Scalability of Quad Interface p-MTJ for 1X nm STT-MRAM With 10-ns Low Power Write Operation, 10 Years Retention and Endurance > 10Â¹Â¹. IEEE Transactions on Electron Devices, 2020, 67, 5368-5373.	3.0	26
20	A Systematic Study of Tiny YOLO3 Inference: Toward Compact Brainware Processor With Less Memory and Logic Gate. IEEE Access, 2020, 8, 142931-142955.	4.2	15
21	Recent Progresses in STT-MRAM and SOT-MRAM for Next Generation MRAM. , 2020, , .		18
22	Influence of Hard Mask Materials on the Magnetic Properties of Perpendicular MTJs With Double CoFeB/MgO Interface. IEEE Transactions on Magnetics, 2020, 56, 1-4.	2.1	6
23	Micromagnetic simulation of the temperature dependence of the switching energy barrier using string method assuming sidewall damages in perpendicular magnetized magnetic tunnel junctions. AIP Advances, 2020, 10, .	1.3	10
24	FPGA Implementation of Real-Time Pedestrian Detection Using Normalization-Based Validation of Adaptive Features Clustering. IEEE Transactions on Vehicular Technology, 2020, 69, 9330-9341.	6.3	13
25	Novel Quad-Interface MTJ Technology and its First Demonstration With High Thermal Stability Factor and Switching Efficiency for STT-MRAM Beyond 2X nm. IEEE Transactions on Electron Devices, 2020, 67, 995-1000.	3.0	19
26	Magnetic properties of Co film in Pt/Co/Cr2O3/Pt structure. AIP Advances, 2020, 10, .	1.3	6
27	Normalization-Based Validity Index of Adaptive K-Means Clustering for Multi-Solution Application. IEEE Access, 2020, 8, 9403-9419.	4.2	11
28	A 47.14-$muext{W}$ 200-MHz MOS/MTJ-Hybrid Nonvolatile Microcontroller Unit Embedding STT-MRAM and FPGA for IoT Applications. IEEE Journal of Solid-State Circuits, 2019, 54, 2991-3004.	5.4	39
29	Novel Quad interface MTJ technology and its first demonstration with high thermal stability and switching efficiency for STT-MRAM beyond 2Xnm. , 2019, , .		22
30	Effect of surface modification treatment of buffer layer on thermal tolerance of synthetic ferrimagnetic reference layer in perpendicular-anisotropy magnetic tunnel junctions. Journal of Applied Physics, 2019, 126, .	2.5	7
31	Change in chemical bonding state by thermal treatment in MgO-based magnetic tunnel junction observed by angle-resolved hard X-ray photoelectron spectroscopy. Journal of Applied Physics, 2019, 125, .	2.5	6
32	Oxidation-induced stress in Si nanopillars. Journal of Materials Science, 2019, 54, 11117-11126.	3.7	5
33	Edge effect in the oxidation of three-dimensional nano-structured silicon. Materials Science in Semiconductor Processing, 2019, 93, 266-273.	4.0	10
34	Insertion Layer Thickness Dependence of Magnetic and Electrical Properties for Double-CoFeB/MgO-Interface Magnetic Tunnel Junctions. IEEE Transactions on Magnetics, 2019, 55, 1-4.	2.1	12
35	Variance Reduction during the Fabrication of Sub-20 nm Si Cylindrical Nanopillars for Vertical Gate-All-Around Metal-Oxide-Semiconductor Field-Effect Transistors. ACS Omega, 2019, 4, 21115-21121.	3.5	6
36	A novel memory test system with an electromagnet for STT-MRAM testing. , 2019, , .		1

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37	Effect of capping layer material on thermal tolerance of magnetic tunnel junctions with MgO/CoFeB-based free layer/MgO/capping layers. AIP Advances, 2019, 9, .	1.3	3
38	Novel Method of Evaluating Accurate Thermal Stability for MTJs Using Thermal Disturbance and its Demonstration for Single-/Double-Interface p-MTJ. IEEE Transactions on Magnetics, 2018, 54, 1-5.	2.1	7
39	A Recent Progress of Spintronics Devices for Integrated Circuit Applications. Journal of Low Power Electronics and Applications, 2018, 8, 44.	2.0	48
40	14ns write speed 128Mb density Embedded STT-MRAM with endurance>10¹⁰ and 10yrs retention@85Â°C using novel low damage MTJ integration process. , 2018, , .		33
41	High thermal tolerance synthetic ferrimagnetic reference layer with modified buffer layer by ion irradiation for perpendicular anisotropy magnetic tunnel junctions.. , 2018, , .		0
42	STEM tomography study on structural features induced by MTJ processing. Applied Physics A: Materials Science and Processing, 2018, 124, 1.	2.3	4
43	Etch Process Technology for High Density STT-MRAM. , 2018, , .		3
44	Origin of variation of shift field via annealing at 400Â°C in a perpendicular-anisotropy magnetic tunnel junction with [Co/Pt]-multilayers based synthetic ferrimagnetic reference layer. AIP Advances, 2017, 7, .	1.3	9
45	Impact of Tungsten Sputtering Condition on Magnetic and Transport Properties of Double-MgO Magnetic Tunneling Junction With CoFeB/W/CoFeB Free Layer. IEEE Transactions on Magnetics, 2017, 53, 1-4.	2.1	17
46	Embedded nonvolatile memory with STT-MRAMs and its application for nonvolatile brain-inspired VLSIs. , 2017, , .		0
47	Embedded nonvolatile memory with STT-MRAMs and its application for nonvolatile brain-inspired VLSIs. , 2017, , .		2
48	Impact of sputtering condition for tungsten on magnetic and transport properties of magnetic tunneling junction with CoFeB/W/CoFeB free layer. , 2017, , .		0
49	Stochastic behavior-considered VLSI CAD environment for MTJ/MOS-hybrid microprocessor design. , 2016, , .		4
50	An Overview of Nonvolatile Emerging Memoriesâ€" Spintronics for Working Memories. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2016, 6, 109-119.	3.6	121
51	Standby-Power-Free Integrated Circuits Using MTJ-Based VLSI Computing. Proceedings of the IEEE, 2016, 104, 1844-1863.	21.3	102
52	Demonstration of Yield Improvement for On-Via MTJ Using a 2-Mbit 1T-1MTJ STT-MRAM Test Chip. , 2016, , .		9
53	Improvement of Thermal Tolerance of CoFeBâ€"MgO Perpendicular-Anisotropy Magnetic Tunnel Junctions by Controlling Boron Composition. IEEE Transactions on Magnetics, 2016, 52, 1-4.	2.1	17
54	Effect of series resistance on dielectric breakdown phenomenon of silicon carbide MOS capacitor. , 2015, , .		2

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55	Low-frequency noise reduction in vertical MOSFETs having tunable threshold voltage fabricated with 60 nm CMOS technology on 300 mm wafer process. Japanese Journal of Applied Physics, 2015, 54, 04DC11.	1.5	22
56	Diffusion behaviors observed on the surface of CoFeB film after the natural oxidation and the annealing. , 2015, , .		0
57	1T1MTJ STT-MRAM Cell Array Design with an Adaptive Reference Voltage Generator for Improving Device Variation Tolerance. , 2015, , .		13
58	Driving Force in Diffusion and Redistribution of Reducing Agents During Redox Reaction on the Surface of CoFeB Film. IEEE Transactions on Magnetics, 2015, 51, 1-4.	2.1	1
59	STT-MRAM for low power systems. , 2015, , .		0
60	Evidence of a reduction reaction of oxidized iron/cobalt by boron atoms diffused toward naturally oxidized surface of CoFeB layer during annealing. Applied Physics Letters, 2015, 106, 142407.	3.3	11
61	Fabrication of a 3000-6-input-LUTs embedded and block-level power-gated nonvolatile FPGA chip using p-MTJ-based logic-in-memory structure. , 2015, , .		6
62	Challenge of MTJ-based nonvolatile logic-in-memory architecture for ultra low-power and highly dependable VLSI computing. , 2015, , .		2
63	Nonvolatile Logic-in-Memory LSI Using Cycle-Based Power Gating and its Application to Motion-Vector Prediction. IEEE Journal of Solid-State Circuits, 2015, 50, 476-489.	5.4	53
64	Dependence of Sub-Volume Excitation on Structural and Material Parameters in Precessional Regime of Spin Transfer Torque Magnetization Reversal. IEEE Transactions on Magnetics, 2014, 50, 1-4.	2.1	4
65	Perpendicular-anisotropy CoFeB-MgO based magnetic tunnel junctions scaling down to 1X nm. , 2014, , .		20
66	Studies on read-stability and write-ability of fast access STT-MRAMs. , 2014, , .		5
67	Trend of tunnel magnetoresistance and variation in threshold voltage for keeping data load robustness of metalâ€“oxideâ€“semiconductor/magnetic tunnel junction hybrid latches. Journal of Applied Physics, 2014, 115, 17C728.	2.5	12
68	Influence of hydrogen patterning gas on electric and magnetic properties of perpendicular magnetic tunnel junctions. Journal of Applied Physics, 2014, 115, 17C727.	2.5	10
69	Design of an energy-efficient 2T-2MTJ nonvolatile TCAM based on a parallel-serial-combined search scheme. IEICE Electronics Express, 2014, 11, 20131006-20131006.	0.8	9
70	Complementary 5T-4MTJ nonvolatile TCAM cell circuit with phase-selective parallel writing scheme. IEICE Electronics Express, 2014, 11, 20140297-20140297.	0.8	7
71	An MTJ-based nonvolatile associative memory architecture with intelligent power-saving scheme for high-speed low-power recognition applications. , 2013, , .		2
72	A 1-Mb STT-MRAM with zero-array standby power and 1.5-ns quick wake-up by 8-b fine-grained power gating. , 2013, , .		5

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73	A High Performance Current Latch Sense Amplifier with Vertical MOSFET. IEICE Transactions on Electronics, 2013, E96.C, 655-662.	0.6	1
74	Six-input lookup table circuit with 62% fewer transistors using nonvolatile logic-in-memory architecture with series/parallel-connected magnetic tunnel junctions. Journal of Applied Physics, 2012, 111, .	2.5	51
75	Design of a 270ps-access 7-transistor/2-magnetic-tunnel-junction cell circuit for a high-speed-search nonvolatile ternary content-addressable memory. Journal of Applied Physics, 2012, 111, 07E336.	2.5	23
76	Low Power Nonvolatile Counter Unit with Fine-Grained Power Gating. IEICE Transactions on Electronics, 2012, E95.C, 854-859.	0.6	0
77	Fabrication of Silicon Pillar with 25 nm Half Pitch Using New Multiple Double Patterning Technique. Japanese Journal of Applied Physics, 2011, 50, 04DA16.	1.5	3
78	The Impact of Current Controlled-MOS Current Mode Logic/Magnetic Tunnel Junction Hybrid Circuit for Stable and High-Speed Operation. IEICE Transactions on Electronics, 2011, E94-C, 743-750.	0.6	0
79	Magnetic tunnel junction for nonvolatile CMOS logic. , 2010, , .		66
80	Beyond MRAM: Nonvolatile Logic-in-Memory VLSI. , 0, , 199-230.		1