Daehyun Kim

List of Publications by Year
in descending order

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15 papers	117 citations	1684188 5 h-index	1588992 8 g-index
15 all docs	15 docs citations	15 times ranked	97 citing authors

#	Article	IF	Citations
1	MONETA: A Processing-In-Memory-Based Hardware Platform for the Hybrid Convolutional Spiking Neural Network With Online Learning. Frontiers in Neuroscience, 2022, 16, 775457.	2.8	3
2	ScieNet: Deep learning with spike-assisted contextual information extraction. Pattern Recognition, 2021, 118, 108002.	8.1	5
3	An SRAM Compiler for Monolithic-3D Integrated Circuit with Carbon Nanotube Transistors. IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, 2021, , 1-1.	1.5	1
4	Genetic Algorithm-Based Energy-Aware CNN Quantization for Processing-In-Memory Architecture. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2021, 11, 649-662.	3.6	5
5	SAFE-DNN: A Deep Neural Network With Spike Assisted Feature Extraction For Noise Robust Inference. , 2020, , .		3
6	Processing-In-Memory-Based On-Chip Learning With Spike-Time-Dependent Plasticity in 65-nm CMOS. IEEE Solid-State Circuits Letters, 2020, 3, 278-281.	2.0	9
7	Flex-PIM: A Ferroelectric FET based Vector Matrix Multiplication Engine with Dynamical Bitwidth and Floating Point Precision. , 2020, , .		4
8	Q-PIM: A Genetic Algorithm based Flexible DNN Quantization Method and Application to Processing-In-Memory Platform. , 2020, , .		13
9	Advances in Design and Test of Monolithic 3-D ICs. IEEE Design and Test, 2020, 37, 92-100.	1.2	6
10	A Flexible Precision Multi-Format In-Memory Vector Matrix Multiplication Engine in 65 nm CMOS With RF Machine Learning Support. IEEE Solid-State Circuits Letters, 2020, 3, 450-453.	2.0	2
11	A Heterogeneous Spiking Neural Network for Unsupervised Learning of Spatiotemporal Patterns. Frontiers in Neuroscience, 2020, 14, 615756.	2.8	13
12	RTL-to-GDS design tools for monolithic 3D ICs. , 2020, , .		4
13	A Ferroelectric FET-Based Processing-in-Memory Architecture for DNN Acceleration. IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, 2019, 5, 113-122.	1.5	40
14	RTL-to-GDS Tool Flow and Design-for-Test Solutions for Monolithic 3D ICs. , 2019, , .		8
15	A ReRAM Memory Compiler with Layout-Precise Performance Evaluation. , 2019, , .		1