Changhwan Shin

List of Publications by Year
in descending order

145 papers	2,354 citations	236833 25 h-index	265120 42 g-index
145 all docs	145 docs citations	145 times ranked	2054 citing authors

#	Article	IF	Citations
1	Negative Capacitance Field Effect Transistor With Hysteresis-Free Sub-60-mV/Decade Switching. IEEE Electron Device Letters, 2016, 37, 245-248.	2.2	184
2	Negative Capacitance in Organic/Ferroelectric Capacitor to Implement Steep Switching MOS Devices. Nano Letters, 2015, 15, 4553-4556.	4.5	162
3	Negative Capacitance FinFET With Sub-20-mV/decade Subthreshold Slope and Minimal Hysteresis of 0.48 V. IEEE Electron Device Letters, 2017, 38, 418-421.	2.2	100
4	Vertical Tunnel FET: Design Optimization With Triple Metal-Gate Layers. IEEE Transactions on Electron Devices, 2016, 63, 5030-5035.	1.6	90
5	Ultra-thick semi-crystalline photoactive donor polymer for efficient indoor organic photovoltaics. Nano Energy, 2019, 58, 466-475.	8.2	79
6	Feedback FET: A novel transistor exhibiting steep switching behavior at low bias voltages. , 2008, , .		72
7	Effect of the Si/TiO₂/BiVO₄ Heterojunction on the Onset Potential of Photocurrents for Solar Water Oxidation. ACS Applied Materials & Interfaces, 2015, 7, 5788-5796.	4.0	60
8	Steep switching devices for low power applications: negative differential capacitance/resistance field effect transistors. Nano Convergence, 2018, 5, 2.	6.3	60
9	Tri-Gate Bulk MOSFET Design for CMOS Scaling to the End of the Roadmap. IEEE Electron Device Letters, 2008, 29, 491-493.	2.2	59
10	Sub-60-mV/decade Negative Capacitance FinFET With Sub-10-nm Hafnium-Based Ferroelectric Capacitor. IEEE Journal of the Electron Devices Society, 2017, 5, 306-309.	1.2	57
11	Impact of temperature on negative capacitance fieldâ€effect transistor. Electronics Letters, 2015, 51, 106-108.	0.5	42
12	Study of Random Variation in Germanium-Source Vertical Tunnel FET. IEEE Transactions on Electron Devices, 2016, 63, 1827-1834.	1.6	42
13	Ferroelectric Fieldâ€Effectâ€Transistor Integrated with Ferroelectrics Heterostructure. Advanced Science, 2022, 9, e2200566.	5.6	42
14	Recent Studies on Supercapacitors with Next-Generation Structures. Micromachines, 2020, 11, 1125.	1.4	41
15	Performance and Area Scaling Benefits of FD-SOI Technology for 6-T SRAM Cells at the 22-nm Node. IEEE Transactions on Electron Devices, 2010, 57, 1301-1309.	1.6	40
16	A New Slit-Type Vacuum-Channel Transistor. IEEE Transactions on Electron Devices, 2014, 61, 4186-4191.	1.6	38
17	Effective Schottky Barrier Height Lowering of Metal/n-Ge with a TiO₂/GeO₂ Interlayer Stack. ACS Applied Materials & Interfaces, 2016, 8, 35419-35425.	4.0	37
18	Study of High-k/Metal-Gate Work-Function Variation Using Rayleigh Distribution. IEEE Electron Device Letters, 2013, 34, 532-534.	2.2	36

#	Article	IF	Citations
19	Study of Work-Function Variation in High-<inline-formula> <tex-math notation="LaTeX">$kappa $ </tex-math> </inline-formula>/Metal-Gate Gate-All-Around Nanowire MOSFET. IEEE Transactions on Electron Devices, 2016, 63, 3338-3341.	1.6	36
20	Current-Voltage Model for Negative Capacitance Field-Effect Transistors. IEEE Electron Device Letters, 2017, 38, 669-672.	2.2	36
21	Specific Contact Resistivity Reduction Through Ar Plasma-Treated TiO_{2â^'x} Interfacial Layer to Metal/Ge Contact. IEEE Electron Device Letters, 2014, 35, 1076-1078.	2.2	34
22	Impact of Current Flow Shape in Tapered (Versus Rectangular) FinFET on Threshold Voltage Variation Induced by Work-Function Variation. IEEE Transactions on Electron Devices, 2014, 61, 2007-2011.	1.6	33
23	Steep Slope Silicon-On-Insulator Feedback Field-Effect Transistor: Design and Performance Analysis. IEEE Transactions on Electron Devices, 2019, 66, 286-291.	1.6	33
24	Design Optimization of Multigate Bulk MOSFETs. IEEE Transactions on Electron Devices, 2013, 60, 28-33.	1.6	31
25	Experimental observation of voltage amplification using negative capacitance for sub-60 mV/decade CMOS devices. Current Applied Physics, 2015, 15, 352-355.	1.1	29
26	Symmetric tunnel field-effect transistor (S-TFET). Current Applied Physics, 2015, 15, 71-77.	1.1	28
27	Impact of Equivalent Oxide Thickness on Threshold Voltage Variation Induced by Work-Function Variation in Multigate Devices. IEEE Transactions on Electron Devices, 2017, 64, 2452-2456.	1.6	27
28	Adjusting the Operating Voltage of an Nanoelectromechanical Relay Using Negative Capacitance. IEEE Transactions on Electron Devices, 2017, 64, 5270-5273.	1.6	25
29	Study of High-k/Metal-Gate Work Function Variation in FinFET: The Modified RGG Concept. IEEE Electron Device Letters, 2013, 34, 1560-1562.	2.2	24
30	Transient Response of Negative Capacitance in P(VDF_{0.75}-TrFE_{0.25}) Organic Ferroelectric Capacitor. IEEE Journal of the Electron Devices Society, 2017, 5, 232-236.	1.2	24
31	Silver Nanowire/Colorless-Polyimide Composite Electrode: Application in Flexible and Transparent Resistive Switching Memory. Scientific Reports, 2017, 7, 3438.	1.6	24
32	Performance and Yield Benefits of Quasi-Planar Bulk CMOS Technology for 6-T SRAM at the 22-nm Node. IEEE Transactions on Electron Devices, 2011, 58, 1846-1854.	1.6	23
33	Surface Passivation of Germanium Using SF₆ Plasma to Reduce Source/Drain Contact Resistance in Germanium n-FET. IEEE Electron Device Letters, 2015, 36, 745-747.	2.2	23
34	Variation-Aware Advanced CMOS Devices and SRAM. Springer Series in Advanced Microelectronics, 2016, , .	0.3	23
35	Analytical Study of Interfacial Layer Doping Effect on Contact Resistivity in Metal-Interfacial Layer-Ge Structure. IEEE Electron Device Letters, 2014, 35, 705-707.	2.2	22
36	Random Variation Analysis and Variation-Aware Design of Symmetric Tunnel Field-Effect Transistor. IEEE Transactions on Electron Devices, 2015, 62, 1778-1783.	1.6	21

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37	Polarity control in a single transition metal dichalcogenide (TMD) transistor for homogeneous complementary logic circuits. Nanoscale, 2019, 11, 12871-12877.	2.8	21
38	Study of Work-Function Variation for High-<inline-formula> <tex-math notation="LaTeX">$kappa $ </tex-math></inline-formula>/Metal-Gate Ge-Source Tunnel Field-Effect Transistors. IEEE Transactions on Electron Devices, 2015, 62, 2143-2147.	1.6	20
39	Study of a hysteresis window of FinFET and fully-depleted silicon-on-insulator (FDSOI) MOSFET with ferroelectric capacitor. Nano Convergence, 2020, 7, 19.	6.3	20
40	The Efficacy of Metal-Interfacial Layer-Semiconductor Source/Drain Structure on Sub-10-nm n-Type Ge FinFET Performances. IEEE Electron Device Letters, 2014, 35, 1185-1187.	2.2	19
41	3-D Quasi-Atomistic Model for Line Edge Roughness in Nonplanar MOSFETs. IEEE Transactions on Electron Devices, 2016, 63, 4617-4623.	1.6	18
42	Performance Booster for Vertical Tunnel Field-Effect Transistor: Field-Enhanced High- $kappa $ Layer. IEEE Electron Device Letters, 2016, 37, 1383-1386.	2.2	16
43	Design for Variation-Immunity in Sub-10-nm Stacked-Nanowire FETs to Suppress LER-induced Random Variations. IEEE Transactions on Electron Devices, 2016, 63, 5048-5054.	1.6	15
44	Machine Learning (ML)-Based Model to Characterize the Line Edge Roughness (LER)-Induced Random Variation in FinFET. IEEE Access, 2020, 8, 158237-158242.	2.6	15
45	Understanding of Feedback Field-Effect Transistor and Its Applications. Applied Sciences (Switzerland), 2020, 10, 3070.	1.3	15
46	Random Dopant Fluctuation-Induced Threshold Voltage Variation-Immune Ge FinFET With Metalâ€“Interlayerâ€“Semiconductor Source/Drain. IEEE Transactions on Electron Devices, 2016, 63, 4167-4172.	1.6	14
47	Fermi-Level Unpinning Technique with Excellent Thermal Stability for n-Type Germanium. ACS Applied Materials & Interfaces, 2017, 9, 35988-35997.	4.0	14
48	Analysis on the Operation of Negative Differential Resistance FinFET With Pb(Zr_{0.52}Ti_{0.48})O₃ Threshold Selector. IEEE Transactions on Electron Devices, 2018, 65, 19-22.	1.6	13
49	Analysis of Random Variations and Variation-Robust Advanced Device Structures. Journal of Semiconductor Technology and Science, 2014, 14, 8-22.	0.1	13
50	Fermi-Level Unpinning Using a Ge-Passivated Metalâ€“Interlayerâ€“Semiconductor Structure for Non-Alloyed Ohmic Contact of High-Electron-Mobility Transistors. IEEE Electron Device Letters, 2015, 36, 884-886.	2.2	12
51	Program/Erase Scheme for Suppressing Interface Trap Generation in HfO₂-Based Ferroelectric Field Effect Transistor. IEEE Electron Device Letters, 2021, 42, 1280-1283.	2.2	12
52	Effect of Hydrogen Annealing on Contact Resistance Reduction of Metalâ€“Interlayerâ€“n-Germanium Source/Drain Structure. IEEE Electron Device Letters, 2016, , 1-1.	2.2	11
53	Impact of the Metal-Gate Material Properties in FinFET (Versus FD-SOI MOSFET) on High-<inline-formula> <tex-math notation="LaTeX">$kappa$ </tex-math> </inline-formula>/Metal-Gate Work-Function Variation. IEEE Transactions on Electron Devices, 2018, 65, 4780-4785.	1.6	11
54	Device design guideline for junctionless gate-all-around nanowire negative-capacitance FET with HfO₂-based ferroelectric gate stack. Semiconductor Science and Technology, 2020, 35, 015011.	1.0	11

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55	Influence of High-Pressure Annealing on Memory Properties of Hf_{0.5}Zr_{0.5}O₂ Based 1T-FeRAM. IEEE Electron Device Letters, 2019, 40, 1076-1079.	2.2	10
56	DIBL enhancement in ferroelectric-gated FinFET. Semiconductor Science and Technology, 2019, 34, 025004.	1.0	10
57	Understanding of Polarization-Induced Threshold Voltage Shift in Ferroelectric-Gated Field Effect Transistor for Neuromorphic Applications. Electronics (Switzerland), 2020, 9, 704.	1.8	10
58	Impact of Chamber/Annealing Temperature on the Endurance Characteristic of Zr:HfO2 Ferroelectric Capacitor. Sensors, 2022, 22, 4087.	2.1	10
59	Comparative study in work-function variation: Gaussian vs. Rayleigh distribution for grain size. IEICE Electronics Express, 2013, 10, 20130109-20130109.	0.3	9
60	Transconductance Amplification by the Negative Capacitance in Ferroelectric-Gated P3HT Thin-Film Transistor. IEEE Transactions on Electron Devices, 2017, 64, 4974-4979.	1.6	9
61	Comprehensive study of high pressure annealing on the ferroelectric properties of Hf_{0.5}Zr_{0.5}O₂ thin films. Nanotechnology, 2019, 30, 505204.	1.3	9
62	Gate-induced drain leakage (GIDL) in MFMIS and MFIS negative capacitance FinFETs. Current Applied Physics, 2020, 20, 1222-1225.	1.1	9
63	NCFET-Based 6-T SRAM: Yield Estimation Based on Variation-Aware Sensitivity. IEEE Journal of the Electron Devices Society, 2020, 8, 182-188.	1.2	9
64	Probabilistic Artificial Neural Network for Line-Edge-Roughness-Induced Random Variation in FinFET. IEEE Access, 2021, 9, 86581-86589.	2.6	9
65	Super steep-switching (SS â‰ˆ 2 mV/decade) phase-FinFET with Pb(Zr0.52Ti0.48)O3 threshold switching device. Applied Physics Letters, 2018, 113, .	1.5	8
66	Negative Capacitance Transistor with Twoâ€Ðimensional Channel Material (Molybdenum disulfide,) Tj ETQq0 0 0 rgBT /Overlock 10 Tf 5	0.8	8
67	Ferroelectric-Gated Nanoelectromechanical Nonvolatile Memory Cell. IEEE Transactions on Electron Devices, 2019, 66, 407-412.	1.6	8
68	MFMIS Negative Capacitance FinFET Design for Improving Drive Current. Electronics (Switzerland), 2020, 9, 1423.	1.8	8
69	Study on Various Device Structures for Steep-Switching Silicon-on-Insulator Feedback Field-Effect Transistors. IEEE Transactions on Electron Devices, 2020, 67, 1852-1858.	1.6	8
70	Optimization of double metal-gate InAs/Si heterojunction nanowire TFET. Semiconductor Science and Technology, 2020, 35, 075024.	1.0	8
71	Prediction Model for Random Variation in FinFET Induced by Line-Edge-Roughness (LER). Electronics (Switzerland), 2021, 10, 455.	1.8	8
72	Experimental understanding of polarization switching in PZT ferroelectric capacitor. Semiconductor Science and Technology, 2019, 34, 075004.	1.0	7

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73	Experimental observation of zero DIBL in short-channel hysteresis-free ferroelectric-gated FinFET. Solid-State Electronics, 2019, 153, 12-15.	0.8	7
74	Impact of depolarization electric-field and charge trapping on the coercive voltage of an Si:HfO₂-based ferroelectric capacitor. Semiconductor Science and Technology, 2021, 36, 015005.	1.0	7
75	Study on memory characteristics of fin-shaped feedback field effect transistor. Semiconductor Science and Technology, 2022, 37, 065006.	1.0	7
76	Capacitance matching effects in negative capacitnace field effect transistor. , 2016, , .		6
77	Effects of Interface Trap on Transient Negative Capacitance Effect: Phase Field Model. Electronics (Switzerland), 2020, 9, 2141.	1.8	6
78	Impact of Interface Layer on Device Characteristics of Si:HfO₂-Based FeFETâ€™s. IEEE Transactions on Device and Materials Reliability, 2021, 21, 176-182.	1.5	6
79	Functional Encapsulating Structure for Wireless and Immediate Monitoring of the Fluid Penetration. Advanced Functional Materials, 2022, 32, .	7.8	6
80	Experimental demonstration of a ferroelectric FET using paper substrate. IEICE Electronics Express, 2014, 11, 20140447-20140447.	0.3	5
81	State-of-the-art silicon device miniaturization technology and its challenges. IEICE Electronics Express, 2014, 11, 20142005-20142005.	0.3	5
82	Measurement of the quantum capacitance from two-dimensional surface state of a topological insulator at room temperature. Applied Surface Science, 2017, 407, 16-20.	3.1	5
83	Effective drive current in steep slope FinFET (vs. conventional FinFET). Applied Physics Letters, 2017, 111, .	1.5	5
84	Impact of Interface Traps and Surface Roughness on the Device Performance of Stacked-Nanowire FETs. IEEE Transactions on Electron Devices, 2017, 64, 4025-4030.	1.6	5
85	Impact of negative capacitance on the energy-delay property of an electromechanical relay. Japanese Journal of Applied Physics, 2019, 58, 051003.	0.8	5
86	Study of line edge roughness on various types of gate-all-around field effect transistor. Semiconductor Science and Technology, 2020, 35, 015004.	1.0	5
87	Electrical Characteristics of Bulk FinFET According to Spacer Length. Electronics (Switzerland), 2020, 9, 1283.	1.8	5
88	Abruptly-Switching MoSâ‚‚-Channel Atomic-Threshold-Switching Field-Effect Transistor With AgTi/HfOâ‚‚-Based Threshold Switching Device. IEEE Access, 2021, 9, 116953-116961.	2.6	5
89	Tri-gate bulk MOSFET design for improved robustness to random dopant fluctuations. , 2008, , .		4
90	SRAM yield enhancement with thin-BOX FD-SOI. , 2009, , .		4

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91	SRAM cell design considerations for SOI technology. , 2009, , .		4
92	Negative quantum capacitance effect from Bi2Te1.5Se1.5 with frequency dependent capacitance of polyvinyl alcohol (PVA) film in MOS structure. Applied Surface Science, 2019, 463, 1046-1050.	3.1	4
93	External Resistor-Free Gate Configuration Phase Transition FDSOI MOSFET. IEEE Journal of the Electron Devices Society, 2019, 7, 186-190.	1.2	4
94	Device-design optimization of ferroelectric-gated vertical tunnel field-effect transistor to suppress ambipolar current. Semiconductor Science and Technology, 2020, 35, 085010.	1.0	4
95	Study of random dopant fluctuation in PNPN feedback FET. Semiconductor Science and Technology, 2020, 35, 035019.	1.0	4
96	A Soft Pressure Sensor Array Based on a Conducting Nanomembrane. Micromachines, 2021, 12, 933.	1.4	4
97	Inverter design with positive feedback field-effect transistors. Semiconductor Science and Technology, 2022, 37, 035014.	1.0	4
98	SRAM yield and performance enhancements with tri-gate bulk MOSFETs. , 2008, , .		3
99	Full 3D Simulation of 6T-SRAM Cells for the 22nm Node. , 2009, , .		3
100	SRAM design in fully-depleted SOI technology. , 2010, , .		3
101	Performance analysis and optimization for silicon interposer with Through Silicon Via (TSV). , 2012, , .		3
102	Effect of Metal Nitride on Contact Resist ivity of Metal- Interlayer- Ge Source/Drain in Sub- 10 nm ntype Ge FinFET. IEEE Electron Device Letters, 2016, , 1-1.	2.2	3
103	Theoretical study of ferroelectric-gated nanoelectromechanical diode nonvolatile memory cell. Solid-State Electronics, 2020, 163, 107662.	0.8	3
104	Experimental study of interface traps in MOS capacitor with Al-doped HfO₂. Semiconductor Science and Technology, 2020, 35, 085029.	1.0	3
105	Compact model for PZT ferroelectric capacitors with voltage dependent switching behavior. Semiconductor Science and Technology, 2020, 35, 055033.	1.0	3
106	Energy-Delay Sensitivity Analysis of a Nanoelectromechanical Relay With the Negative Capacitance of a Ferroelectric Capacitor. IEEE Journal of the Electron Devices Society, 2020, 8, 365-372.	1.2	3
107	Worst Case Sampling Method with Confidence Ellipse for Estimating the Impact of Random Variation on Static Random Access Memory (SRAM). Journal of Semiconductor Technology and Science, 2015, 15, 374-380.	0.1	3
108	Design of JL-CFET (junctionless complementary field effect transistor)-based inverter for low power applications. Semiconductor Science and Technology, 2022, 37, 035019.	1.0	3

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109	The design optimization and variation study of segmented-channel MOSFET using HfO<inf>2</inf> or SiO<inf>2</inf> trench isolation. , 2013, , .		2
110	Effect of double-patterning and double-etching on the line-edge-roughness of multi-gate bulk MOSFETs. IEICE Electronics Express, 2013, 10, 20130108-20130108.	0.3	2
111	Worst Case Sampling Method to Estimate the Impact of Random Variation on Static Random Access Memory. IEEE Transactions on Electron Devices, 2015, 62, 1705-1709.	1.6	2
112	Tunnel Field-Effect Transistor With Segmented Channel. IEEE Journal of the Electron Devices Society, 2019, 7, 621-625.	1.2	2
113	DIBL improvement in hysteresis-free and ferroelectric-gated FinFETs. Semiconductor Science and Technology, 2019, 34, 065001.	1.0	2
114	Experimental study of threshold voltage shift for Si:HfO2 based ferroelectric field effect transistor. Nanotechnology, 2021, 32, 375203.	1.3	2
115	Impact of the double-patterning technique on the LER-induced threshold voltage variation in symmetric tunnel field-effect transistor. IEICE Electronics Express, 2015, 12, 20150349-20150349.	0.3	1
116	Amorphous Indium Zinc Oxide Thin-Film Transistor with Steep Subthreshold Slope by Negative Capacitance. IEICE Transactions on Electronics, 2016, E99.C, 544-546.	0.3	1
117	Simulation Techniques for Nanoelectromechanical (NEM) Relay. Journal of Nanoscience and Nanotechnology, 2018, 18, 6615-6618.	0.9	1
118	Study of work-function variation in stacked multiple-channel-structure device. Semiconductor Science and Technology, 2019, 34, 125003.	1.0	1
119	Process-Induced Random Variation: Work-Function Variation in Stacked Nanowire Field Effect Transistor. Journal of Nanoscience and Nanotechnology, 2019, 19, 6091-6094.	0.9	1
120	Steep Slope Silicon-on-Insulator Field Effect Transistor with Negative Capacitance: Analysis on Hysteresis. Journal of Nanoscience and Nanotechnology, 2019, 19, 6128-6130.	0.9	1
121	Time-resolved electrical characteristics of ferroelectric-gated fully depleted silicon on insulator devices. Solid-State Electronics, 2020, 164, 107698.	0.8	1
122	Endurance of ferroelectric La-doped HfO2 for SFS gate-stack memory devices. , 2020, , .		1
123	Investigation on Threshold Voltage Adjustment of Threshold Switching Devices with HfO2/Al2O3 Superlattice on Transparent ITO/Glass Substrate. Micromachines, 2020, 11, 525.	1.4	1
124	Steep-Switching Fully Depleted Silicon-on-Insulator (FDSOI) Phase-Transition Field-Effect Transistor With Optimized HfOâ„/Alâ„Oâ„ƒ-Multilayer-Based Threshold Switching Device. IEEE Transactions on Electron Devices, 2021, 68, 1358-1363.	1.6	1
125	LER-Induced Random Variationâ€“Immune Effect of Metal-Interlayerâ€“Semiconductor Source/Drain Structure on N-Type Ge Junctionless FinFETs. IEEE Transactions on Electron Devices, 2021, 68, 1340-1345.	1.6	1
126	Impact of Rapid-Thermal-Annealing Temperature on the Polarization Characteristics of a PZT-Based Ferroelectric Capacitor. Electronics (Switzerland), 2021, 10, 1324.	1.8	1

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127	Gate-Stack Engineering to Improve the Performance of 28 nm Low-Power High-K/Metal-Gate Device. Micromachines, 2021, 12, 886.	1.4	1
128	Performance analysis and yield estimation for a negative capacitance field effect transistor-based eight-transistor static random access memory. Semiconductor Science and Technology, 2021, 36, 095028.	1.0	1
129	Quantitative evaluation of process-induced line-edge roughness in FinFET: Bayesian regression model. Semiconductor Science and Technology, 2021, 36, 025020.	1.0	1
130	Comparative Study of Negative Capacitance in Ferroelectric Capacitors : P(VDF0.75-TrFE0.25) Versus Pb(Zr, Ti)Oâ‚ƒ. Journal of Semiconductor Technology and Science, 2018, 18, 167-171.	0.1	1
131	Comparative Study of Negative Differential Capacitance in Ferroelectric Capacitors: P(VDF0.75-TrFE0.25) and P(VDF0.50-TrFE0.50). Journal of Semiconductor Technology and Science, 2018, 18, 321-327.	0.1	1
132	Quantitative Evaluation of Line-Edge Roughness in Various FinFET Structures: Bayesian Neural Network With Automatic Model Selection. IEEE Access, 2022, 10, 26340-26346.	2.6	1
133	Strain-Dependent Photoacoustic Characteristics of Free-Standing Carbon-Nanocomposite Transmitters. Sensors, 2022, 22, 3432.	2.1	1
134	Analysis and modeling for random telegraph noise of GIDL current in saddle MOSFET for DRAM application. IEICE Electronics Express, 2014, 11, 20140468-20140468.	0.3	0
135	Design Optimization for Process-Variation-Tolerant 22-nm FinFET-Based 6-T SRAM Cell with Worst-Case Sampling Method. IEICE Transactions on Electronics, 2016, E99.C, 541-543.	0.3	0
136	Layout engineering to suppress hysteresis of negative capacitance FinFET. , 2017, , .		0
137	Impact of Ferroelectric Capacitorâ€™s Electrode Area on the Performance of Negative Capacitance Field Effect Transistor. Journal of Nanoscience and Nanotechnology, 2019, 19, 6087-6090.	0.9	0
138	Precise control of nanoscale spacing between electrodes using different natured self-assembled monolayers. Nanotechnology, 2019, 30, 265302.	1.3	0
139	Device Design Guideline for HfOâ‚‚-Based Ferroelectric-Gated Nanoelectromechanical System. IEEE Journal of the Electron Devices Society, 2020, 8, 608-613.	1.2	0
140	Electrical Characteristics of Nanoelectromechanical Relay with Multi-Domain HfO2-Based Ferroelectric Materials. Electronics (Switzerland), 2020, 9, 1208.	1.8	0
141	FBFET (Feedback Field Effect Transistor)-based oscillator for neuromorphic computing. Semiconductor Science and Technology, 0, , .	1.0	0
142	CMOS Device Design with Ferroelectric Materials. , 2021, , .		0
143	Impact of Process-Induced Variations on Negative Capacitance Junctionless Nanowire FET. Electronics (Switzerland), 2021, 10, 1899.	1.8	0
144	Experimental Observation of Negative Capacitance in Organic/Ferroelectric Capacitor for Steep Switching MOSFET. Journal of Nanoscience and Nanotechnology, 2017, 17, 3469-3471.	0.9	0

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145	Impact of Stacking-Up and Scaling-Down Bit Cells in 3D NAND on Their Threshold Voltages. Micromachines, 2022, 13, 1139.	1.4	0