Irith Pomeranz

List of Publications by Year in Descending Order

208 papers	906 citations	14 h-index	20 g-index
267 ext. papers	1,210 ext. citations	2.1 avg, IF	5.34 L-index

#	Paper	IF	Citations
208	Wrapping Paths of Undetected Transition Faults with Two-Cycle Gate-Exhaustive Faults. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2022**, 1-1	2.5	
207	Topping Off Test Sets under Bounded Transparent-Scan. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2022**, 1-1	2.5	
206	Pass/Fail Data for Logic Diagnosis under Bounded Transparent-Scan. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2021**, 1-1	2.5	
205	Storage-Based Logic Built-In Self-Test with Multicycle Tests. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2021**, 1-1	2.5	
204	Equivalent Faults under Launch-on-Shift (LOS) Tests with Equal Primary Input Vectors. *ACM Transactions on Design Automation of Electronic Systems*, **2021**, 26, 1-15	1.5	
203	Functional Constraints in the Selection of Two-Cycle Gate-Exhaustive Faults for Test Generation. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2021**, 29, 1500-1504	2.6	
202	Test Compaction by Backward and Forward Extension of Multicycle Tests. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2021**, 29, 242-246	2.6	
201	PRESERVE: Static Test Compaction that Preserves Individual Numbers of Tests. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2021**, 40, 803-807	2.5	0
200	Maximal Independent Fault Set for Gate-Exhaustive Faults. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2021**, 40, 598-602	2.5	4
199	Hybrid Pass/Fail and Full Fail Data for Reduced Fail Data Volume. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2021**, 40, 1711-1720	2.5	2
198	Padding of LFSR Seeds for Reduced Input Test Data Volume. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2021**, 40, 1004-1008	2.5	0
197	GEPDFs: Path Delay Faults Based on Two-Cycle Gate-Exhaustive Faults. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2021**, 1-1	2.5	0
196	Partitioning Functional Test Sequences Into Multicycle Functional Broadside Tests. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2021**, 29, 89-99	2.6	0
195	Efficient Identification of Undetectable Two-Cycle Gate-Exhaustive Faults. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2021**, 1-1	2.5	
194	Static Test Compaction using Independent Suffixes of a Transparent-Scan Sequence. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2021**, 1-1	2.5	
193	Multicycle Tests with Fault Detection Test Data for Improved Logic Diagnosis. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2021**, 1-1	2.5	
192	Single Test Type to Replace Broadside and Skewed-Load Tests for Transition Faults. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2021**, 29, 423-433	2.6	1

191	Logic Diagnosis with Hybrid Fail Data. *ACM Transactions on Design Automation of Electronic Systems*, **2021**, 26, 1-13	1.5	1
190	Broad-Brush Compaction for Sequential Test Generation. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2020**, 28, 1940-1944	2.6	1
189	LFSR-Based Test Generation for Reduced Fail Data Volume. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2020**, 39, 5261-5266	2.5	0
188	RETRO: Reintroducing Tests for Improved Reverse Order Fault Simulation. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2020**, 28, 1930-1934	2.6	
187	Direct Computation of LFSR-Based Stored Tests for Broadside and Skewed-Load Tests. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2020**, 39, 5238-5246	2.5	0
186	Selecting Close-to-Functional Path Delay Faults for Test Generation **2020**,		2
185	Broadside Tests for Transition and Stuck-At Faults. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2020**, 39, 1739-1743	2.5	
184	Globally Functional Transparent-Scan Sequences. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2020**, 39, 3012-3022	2.5	
183	Selection of Primary Output Vectors to Observe Under Multicycle Tests. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2020**, 28, 156-162	2.6	
182	Extra Clocking of LFSR Seeds for Improved Path Delay Fault Coverage. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2020**, 28, 544-552	2.6	2
181	Functional Broadside Tests Under Broadcast Scan. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2020**, 39, 3139-3143	2.5	
180	Input Test Data Volume Reduction Using Seed Complementation and Multiple LFSRs **2020**,		2
179	Non-Masking Non-Robust Tests for Path Delay Faults **2020**,		1
178	. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2020**, 1-1	2.5	1
177	Reverse Low-Power Broadside Tests. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2020**, 39, 742-746	2.5	
176	Switching Activity of Faulty Circuits in Presence of Multiple Transition Faults. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2020**, 39, 936-945	2.5	
175	Multicycle Broadside and Skewed-Load Tests for Test Compaction. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2020**, 39, 262-266	2.5	2
174	New Targets for Diagnostic Test Generation. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2020**, 39, 3035-3043	2.5	

173	Resynthesis for Avoiding Undetectable Faults Based on Design-for-Manufacturability Guidelines **2019**,		1
172	Test Scores for Improving the Accuracy of Logic Diagnosis for Multiple Defects. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2019**, 27, 1720-1724	2.6	2
171	Diagnostic Test Generation That Addresses Diagnostic Holes. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2019**, 38, 335-344	2.5	
170	Test Compaction Under Bounded Transparent-Scan **2019**,		7
169	Padding of Multicycle Broadside and Skewed-Load Tests. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2019**, 27, 2587-2595	2.6	
168	Extended Transparent-Scan. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2019**, 27, 2096-2104	2.6	1
167	Skewed-Load Tests for Transition and Stuck-at Faults. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2019**, 38, 1969-1973	2.5	6
166	Extracting a Close-to-Minimum Multicycle Functional Broadside Test Set From a Functional Test Sequence. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2019**, 27, 1428-1437	2.6	
165	Iterative Test Generation for Gate-Exhaustive Faults to Cover the Sites of Undetectable Target Faults **2019**,		2
164	Test Compaction by Test Removal Under Transparent Scan. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2019**, 27, 496-500	2.6	2
163	Invisible-Scan: A Design-for-Testability Approach for Functional Test Sequences. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2019**, 38, 2357-2365	2.5	
162	LFSR-Based Test Generation for Path Delay Faults. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2019**, 38, 345-353	2.5	5
161	Selecting Functional Test Sequences for Defect Diagnosis. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2018**, 26, 2160-2164	2.6	0
160	Partially Invariant Patterns for LFSR -Based Generation of Close-to-Functional Broadside Tests. *ACM Transactions on Design Automation of Electronic Systems*, **2018**, 23, 1-18	1.5	2
159	An Initialization Process to Support Online Testing Based on Output Comparison for Identical Finite-State Machines. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2018**, 37, 1494-1504	2.5	2
158	Autonomous Multicycle Tests With Low Storage and Test Application Time Overheads. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2018**, 37, 1881-1892	2.5	
157	Improving the Diagnosability of Scan Chain Faults Under Transparent-Scan by Observation Points. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2018**, 37, 1278-1287	2.5	1
156	Observation Points on State Variables for the Compaction of Multicycle Tests. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2018**, 26, 2567-2571	2.6	3

155	Dynamically Determined Preferred Values and a Design-for-Testability Approach for Multiplexer Select Inputs under Functional Test Sequences. *ACM Transactions on Design Automation of Electronic Systems*, **2018**, 23, 1-16	1.5	
154	Static test compaction procedure for large pools of multicycle functional broadside tests. *IET Computers and Digital Techniques*, **2018**, 12, 233-240	0.9	8
153	Improving the Resolution of Multiple Defect Diagnosis by Removing and Selecting Tests **2018**,		5
152	Covering undetected transition fault sites with optimistic unspecified transition faults under multicycle tests **2018**,		3
151	. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2017**, 36, 351-355	2.5	7
150	Restoration-Based Merging of Functional Test Sequences. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2017**, 36, 1739-1749	2.5	0
149	Close-to-Functional Broadside Tests With a Safety Margin. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2017**, 36, 2139-2143	2.5	2
148	Selecting Replacements for Undetectable Path Delay Faults. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2017**, 25, 1988-1992	2.6	3
147	Test Modification for Reduced Volumes of Fail Data. *ACM Transactions on Design Automation of Electronic Systems*, **2017**, 22, 1-17	1.5	3
146	Reordering Tests for Efficient Fail Data Collection and Tester Time Reduction. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2017**, 25, 1497-1505	2.6	1
145	Functional Broadside Test Generation Using a Commercial ATPG Tool **2017**,		2
144	A bridging fault model for line coverage in the presence of undetected transition faults **2017**,		2
143	Clock Sequences for Increasing the Fault Coverage of Functional Test Sequences. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2017**, 36, 1231-1235	2.5	2
142	Reconstruction of a functional test sequence for increased fault coverage. *IET Computers and Digital Techniques*, **2017**, 11, 91-99	0.9	
141	Identifying Biases of a Defect Diagnosis Procedure. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2017**, 36, 1215-1225	2.5	0
140	POSTT: Path-oriented static test compaction for transition faults in scan circuits **2017**,		2
139	Metric for the ability of functional capture cycles to ensure functional operation conditions. *IET Computers and Digital Techniques*, **2017**, 11, 100-106	0.9	
138	Diagnostic Fail Data Minimization Using an N -Cover Algorithm. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2016**, 24, 1198-1202	2.6	1

137	Improving the accuracy of defect diagnosis by adding and removing tests. *IET Computers and Digital Techniques*, **2016**, 10, 47-53	0.9	
136	A Compact Set of Seeds for LFSR-Based Test Generation from a Fully-Specified Compact Test Set **2016**,		2
135	LFSR-Based Generation of Multicycle Tests. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2016**, 1-1	2.5	0
134	Static test compaction for circuits with multiple independent scan chains. *IET Computers and Digital Techniques*, **2016**, 10, 12-17	0.9	1
133	Reduction of diagnostic fail data volume and tester time using a dynamic N-cover algorithm **2016**,		7
132	Balancing the Numbers of Detected Faults for Improved Test Set Quality. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2016**, 35, 337-341	2.5	
131	Improving the Accuracy of Defect Diagnosis with Multiple Sets of Candidate Faults. *IEEE Transactions on Computers*, **2016**, 65, 2332-2338	2.5	2
130	A Test Selection Procedure for Improving the Accuracy of Defect Diagnosis. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2016**, 24, 2759-2767	2.6	7
129	Static Test Compaction for Functional Test Sequences With Restoration of Functional Switching Activity. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2016**, 35, 1755-1762	2.5	
128	$LFSR$ -Based Generation of Partially-Functional Broadside Tests. *IEEE Transactions on Computers*, **2016**, 65, 2659-2664	2.5	4
127	A Joint Diagnostic Test Generation Procedure with Dynamic Test Compaction **2016**,		4
126	Combined input test data volume reduction for mixed broadside and skewed-load test sets. *IET Computers and Digital Techniques*, **2016**, 10, 138-145	0.9	
125	On the Switching Activity in Faulty Circuits During Test Application **2016**,		2
124	A Multicycle Test Set Based on a Two-Cycle Test Set With Constant Primary Input Vectors. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2015**, 34, 1124-1132	2.5	19
123	Use of input necessary assignments for test generation based on merging of test cubes. *IET Computers and Digital Techniques*, **2015**, 9, 106-112	0.9	
122	Improving the accuracy of defect diagnosis by considering reduced diagnostic information **2015**,		2
121	Modeling a Set of Functional Test Sequences as a Single Sequence for Test Compaction. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2015**, 23, 2629-2638	2.6	1
120	Two-Dimensional Static Test Compaction for Functional Test Sequences. *IEEE Transactions on Computers*, **2015**, 64, 3009-3015	2.5	1

119	Generation of close-to-functional broadside tests with equal primary input vectors **2015**,		7
118	Piecewise-Functional Broadside Tests Based on Reachable States. *IEEE Transactions on Computers*, **2015**, 64, 2415-2420	2.5	8
117	Computation of Seeds for LFSR-Based Diagnostic Test Generation. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2015**, 34, 2004-2012	2.5	10
116	Skewed-Load Test Cubes Based on Functional Broadside Tests for a Low-Power Test Set. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2015**, 23, 593-597	2.6	5
115	Computing Seeds for LFSR-Based Test Generation From Nontest Cubes. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2015**, 1-5	2.6	1
114	Test compaction by test cube merging for four-way bridging faults **2015**,		1
113	Test Vector Omission for Fault Coverage Improvement of Functional Test Sequences. *IEEE Transactions on Computers*, **2015**, 64, 3317-3321	2.5	
112	Static Test Compaction for Low-Power Test Sets by Increasing the Switching Activity. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2015**, 23, 1936-1940	2.6	2
111	Test Compaction by Sharing of Functional Test Sequences Among Logic Blocks. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2015**, 23, 3006-3014	2.6	
110	Functional Broadside Tests for Multistep Defect Diagnosis. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2014**, 33, 1429-1433	2.5	1
109	Input Test Data Volume Reduction for Skewed-Load Tests by Additional Shifting of Scan-In States. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2014**, 33, 638-642	2.5	6
108	OBO: An Output-by-Output Scoring Algorithm for Fault Diagnosis **2014**,		17
107	Simultaneous Generation of Functional and Low-Power Non-Functional Broadside Tests. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2014**, 33, 1245-1257	2.5	3
106	Fault simulation with test switching for static test compaction **2014**,		4
105	Selection of Functional Test Sequences With Overlaps. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2014**, 33, 1095-1099	2.5	0
104	Low-Power Diagnostic Test Sets for Transition Faults Based on Functional Broadside Tests. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2014**, 22, 2427-2431	2.6	0
103	Low-Power Test Generation by Merging of Functional Broadside Test Cubes. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2014**, 22, 1570-1582	2.6	9
102	Sharing Logic for Built-In Generationof Functional Broadside Tests. *IEEE Transactions on Computers*, **2014**, 63, 1048-1054	2.5	

101	Unknown Output Values of Faulty Circuits and Output Response Compaction. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2014**, 33, 323-327	2.5	1
100	On the use of multi-cycle tests for storage of two-cycle broadside tests **2014**,		5
99	Reducing the input test data volume under transparent scan. *IET Computers and Digital Techniques*, **2014**, 8, 1-10	0.9	1
98	Multi-cycle broadside tests with runs of constant primary input vectors. *IET Computers and Digital Techniques*, **2014**, 8, 90-96	0.9	1
97	Static Test Compaction for Scan Circuits by Using Restoration to Modify and Remove Tests. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2014**, 33, 1955-1964	2.5	7
96	Improving the Accuracy of Defect Diagnosis by Considering Fewer Tests. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2014**, 33, 2010-2014	2.5	15
95	Restoration-Based Procedures With Set Covering Heuristics for Static Test Compaction of Functional Test Sequences. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2014**, 22, 779-791	2.6	5
94	Test Compaction by Sharing of Transparent-Scan Sequences Among Logic Blocks. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2014**, 22, 792-802	2.6	1
93	Functional Broadside Tests With Incompletely Specified Scan-In States. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2013**, 32, 1445-1449	2.5	5
92	An Adjacent Switching Activity Metric under Functional Broadside Tests. *IEEE Transactions on Computers*, **2013**, 62, 404-410	2.5	3
91	Signal-Transition Patterns of Functional Broadside Tests. *IEEE Transactions on Computers*, **2013**, 62, 2544-2549	2.5	6
90	On Test Compaction of Broadside and Skewed-Load Test Cubes. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2013**, 21, 1705-1714	2.6	8
89	Generation of Functional Broadside Tests for Logic Blocks With Constrained Primary Input Sequences. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2013**, 32, 442-452	2.5	6
88	Built-In Generation of Functional Broadside Tests Using a Fixed Hardware Structure. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2013**, 21, 124-132	2.6	5
87	Reduced Power Transition Fault Test Sets for Circuits With Independent Scan Chain Modes. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2013**, 21, 1354-1359	2.6	3
86	Computing Two-Pattern Test Cubes for Transition Path Delay Faults. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2013**, 21, 475-485	2.6	
85	Broadside and Skewed-Load Tests Under Primary Input Constraints. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2013**, 21, 776-780	2.6	
84	Functional Broadside Templates for Low-Power Test Generation. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2013**, 21, 2321-2325	2.6	1

83	Transition Fault Simulation Considering Broadside Tests as Partially-Functional Broadside Tests. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2013**, 21, 1359-1363	2.6	4
82	Static test compaction for mixed broadside and skewed-load transition fault test sets. *IET Computers and Digital Techniques*, **2013**, 7, 21-28	0.9	2
81	On multi-cycle test cubes. *IET Computers and Digital Techniques*, **2013**, 7, 182-189	0.9	
80	Non-Test Cubes for Test Generation Targeting Hard-to-Detect Faults. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2013**, 32, 1957-1965	2.5	1
79	Concatenation of Functional Test Subsequences for Improved Fault Coverage and Reduced Test Length. *IEEE Transactions on Computers*, **2012**, 61, 899-904	2.5	8
78	Fast Identification of Undetectable Transition Faults under Functional Broadside Tests. *IEEE Transactions on Computers*, **2012**, 61, 905-910	2.5	1
77	On the Switching Activity and Static Test Compaction of Multicycle Scan-Based Tests. *IEEE Transactions on Computers*, **2012**, 61, 1179-1188	2.5	1
76	On the Computation of Common Test Data for Broadside and Skewed-Load Tests. *IEEE Transactions on Computers*, **2012**, 61, 578-583	2.5	15
75	Multipattern Scan-Based Test Sets With Small Numbers of Primary Input Sequences. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2012**, 31, 322-326	2.5	1
74	Non-Uniform Coverage by n-Detection Test Sets. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2012**, 20, 2138-2142	2.6	2
73	Resolution of Diagnosis Based on Transition Faults. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2012**, 20, 172-176	2.6	0
72	On the detection of path delay faults by functional broadside tests **2012**,		4
71	Gradual Diagnostic Test Generation and Observation Point Insertion Based on the Structural Distance Between Indistinguished Fault Pairs. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2012**, 20, 1026-1035	2.6	9
70	A Metric for Identifying Detectable Path Delay Faults. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2012**, 31, 1734-1742	2.5	1
69	Multi-Pattern n-Detection Stuck-At Test Sets for Delay Defect Coverage. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2012**, 20, 1156-1160	2.6	1
68	Multicycle Tests With Constant Primary Input Vectors for Increased Fault Coverage. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2012**, 31, 1428-1438	2.5	8
67	Generation of Mixed Test Sets for Transition Faults. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2012**, 20, 1895-1899	2.6	6
66	Input Necessary Assignments for Testing of Path Delay Faults in Standard-Scan Circuits. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2011**, 19, 333-337	2.6	8

65	Test Strength: A Quality Metric for Transition Fault Tests in Full-Scan Circuits. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2011**, 19, 1907-1911	2.6	
64	Reducing the Storage Requirements of a Test Sequence by Using One or Two Background Vectors. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2011**, 19, 1755-1764	2.6	3
63	Static Test Data Volume Reduction Using Complementation or Modulo-M Addition. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2011**, 19, 1108-1112	2.6	7
62	Generation of Multi-Cycle Broadside Tests. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2011**, 30, 1253-1257	2.5	16
61	Scan Shift Power of Functional Broadside Tests. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2011**, 30, 1416-1420	2.5	5
60	Subsets of Primary Input Vectors in Sequential Test Generation for Single Stuck-at Faults. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2011**, 30, 1579-1583	2.5	0
59	Static test compaction for delay fault test sets consisting of broadside and skewed-load tests **2011**,		23
58	Augmenting Functional Broadside Tests for Transition Fault Coverage with Bounded Switching Activity **2011**,		9
57	Generation of Mixed Broadside and Skewed-Load Diagnostic Test Sets for Transition Faults **2011**,		9
56	On Functional Broadside Tests With Functional Propagation Conditions. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2011**, 19, 1094-1098	2.6	1
55	Built-in generation of functional broadside tests **2011**,		3
54	Broadside and Functional Broadside Tests for Partial-Scan Circuits. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2011**, 19, 1104-1108	2.6	2
53	Hyper-graph based partitioning to reduce DFT cost for pre-bond 3D-IC testing **2011**,		3
52	On reset based functional broadside tests **2010**,		12
51	Forming multi-cycle tests for delay faults by concatenating broadside tests **2010**,		6
50	Selecting state variables for improved on-line testability through output response comparison of identical circuits **2010**,		1
49	Hazard-Based Detection Conditions for Improved Transition Fault Coverage of Scan-Based Tests. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2010**, 18, 333-337	2.6	17
48	Path Selection for Transition Path Delay Faults. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2010**, 18, 401-409	2.6	8

47	Robust Fault Models Where Undetectable Faults Imply Logic Redundancy. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2010**, 18, 1230-1234	2.6	4
46	Switching Activity as a Test Compaction Heuristic for Transition Faults. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2010**, 18, 1357-1361	2.6	9
45	Selection of a Fault Model for Fault Diagnosis Based on Unique Responses. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2010**, 18, 1533-1543	2.6	1
44	Equivalence, Dominance, and Similarity Relations between Fault Pairs and a Fault Pair Collapsing Process for Fault Diagnosis. *IEEE Transactions on Computers*, **2010**, 59, 150-158	2.5	2
43	On Test Generation With Test Vector Improvement. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2010**, 29, 502-506	2.5	14
42	TOV: Sequential Test Generation by Ordering of Test Vectors. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2010**, 29, 454-465	2.5	6
41	On Clustering of Undetectable Single Stuck-At Faults and Test Quality in Full-Scan Circuits. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2010**, 29, 1135-1140	2.5	5
40	Hazard-Based Detection Conditions for Improved Transition Path Delay Fault Coverage. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2010**, 29, 1449-1453	2.5	5
39	On Undetectable Faults and Fault Diagnosis. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2010**, 29, 1832-1837	2.5	
38	Functional and partially-functional skewed-load tests **2010**,		2
37	Output-Dependent Diagnostic Test Generation **2010**,		10
36	On multiple bridging faults **2010**,		1
35	Gradual Diagnostic Test Generation Based on the Structural Distance between Indistinguished Fault Pairs **2010**,		4
34	Random Test Generation With Input Cube Avoidance. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2009**, 17, 45-54	2.6	2
33	Semiconcurrent Online Testing of Transition Faults through Output Response Comparison of Identical Circuits. *IEEE Transactions on Dependable and Secure Computing*, **2009**, 6, 231-240	3.9	
32	Hazard-Based Detection Conditions for Improved Transition Fault Coverage of Functional Test Sequences **2009**,		2
31	Functional Broadside Tests Under an Expanded Definition of Functional Operation Conditions. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2009**, 28, 121-129	2.5	1
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