# Irith Pomeranz

## List of Publications by Citations



| 208 | 906 | 14 | 20 |
|---|---|---|---|
| papers | citations | h-index | g-index |
| 267 | 1,210 | 2.1 | 5.34 |
| ext. papers | ext. citations | avg, IF | L-index |

| # | Paper | IF | Citations |
|---|---|---|---|
| 208 | On static compaction of test sequences for synchronous sequential circuits **1996**, | | 68 |
| 207 | **1992**, | | 58 |
| 206 | Primary Input Vectors to Avoid in Random Test Sequences for Synchronous Sequential Circuits. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2008**, 27, 193-197 | 2.5 | 32 |
| 205 | Static test compaction for delay fault test sets consisting of broadside and skewed-load tests **2011**, | | 23 |
| 204 | Transition Path Delay Faults: A New Path Delay Fault Model for Small and Large Delay Defects. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2008**, 16, 98-107 | 2.6 | 20 |
| 203 | On the generation of scan-based test sets with reachable states for testing under functional operation conditions **2004**, | | 20 |
| 202 | A Multicycle Test Set Based on a Two-Cycle Test Set With Constant Primary Input Vectors. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2015**, 34, 1124-1132 | 2.5 | 19 |
| 201 | OBO: An Output-by-Output Scoring Algorithm for Fault Diagnosis **2014**, | | 17 |
| 200 | Hazard-Based Detection Conditions for Improved Transition Fault Coverage of Scan-Based Tests. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2010**, 18, 333-337 | 2.6 | 17 |
| 199 | Generation of Multi-Cycle Broadside Tests. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2011**, 30, 1253-1257 | 2.5 | 16 |
| 198 | On Selecting Testable Paths in Scan Designs. *Journal of Electronic Testing: Theory and Applications (JETTA)*, **2003**, 19, 447-456 | 0.7 | 16 |
| 197 | On the Computation of Common Test Data for Broadside and Skewed-Load Tests. *IEEE Transactions on Computers*, **2012**, 61, 578-583 | 2.5 | 15 |
| 196 | Improving the Accuracy of Defect Diagnosis by Considering Fewer Tests. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2014**, 33, 2010-2014 | 2.5 | 15 |
| 195 | On Test Generation With Test Vector Improvement. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2010**, 29, 502-506 | 2.5 | 14 |
| 194 | A Functional Coverage Metric for Estimating the Gate-Level Fault Coverage of Functional Tests. *IEEE International Test Conference (TC)*, **2006**, | | 13 |
| 193 | On reset based functional broadside tests **2010**, | | 12 |
| 192 | ATPG Heuristics Dependant Observation Point Insertion for Enhanced Compaction and Data Volume Reduction **2008**, | | 12 |

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| 191 | Estimating the Fault Coverage of Functional Test Sequences Without Fault Simulation **2007**, | | 12 |
| 190 | Unspecified Transition Faults: A Transition Fault Model for At-Speed Fault Simulation and Test Generation. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2008**, 27, 137-146 | 2.5 | 11 |
| 189 | Computation of Seeds for LFSR-Based Diagnostic Test Generation. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2015**, 34, 2004-2012 | 2.5 | 10 |
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| 187 | Low-Power Test Generation by Merging of Functional Broadside Test Cubes. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2014**, 22, 1570-1582 | 2.6 | 9 |
| 186 | Gradual Diagnostic Test Generation and Observation Point Insertion Based on the Structural Distance Between Indistinguished Fault Pairs. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2012**, 20, 1026-1035 | 2.6 | 9 |
| 185 | Switching Activity as a Test Compaction Heuristic for Transition Faults. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2010**, 18, 1357-1361 | 2.6 | 9 |
| 184 | Augmenting Functional Broadside Tests for Transition Fault Coverage with Bounded Switching Activity **2011**, | | 9 |
| 183 | Generation of Mixed Broadside and Skewed-Load Diagnostic Test Sets for Transition Faults **2011**, | | 9 |
| 182 | Piecewise-Functional Broadside Tests Based on Reachable States. *IEEE Transactions on Computers*, **2015**, 64, 2415-2420 | 2.5 | 8 |
| 181 | Concatenation of Functional Test Subsequences for Improved Fault Coverage and Reduced Test Length. *IEEE Transactions on Computers*, **2012**, 61, 899-904 | 2.5 | 8 |
| 180 | On Test Compaction of Broadside and Skewed-Load Test Cubes. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2013**, 21, 1705-1714 | 2.6 | 8 |
| 179 | Multicycle Tests With Constant Primary Input Vectors for Increased Fault Coverage. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2012**, 31, 1428-1438 | 2.5 | 8 |
| 178 | Input Necessary Assignments for Testing of Path Delay Faults in Standard-Scan Circuits. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2011**, 19, 333-337 | 2.6 | 8 |
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| 176 | On Complete Functional Broadside Tests for Transition Faults. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2008**, 27, 583-587 | 2.5 | 8 |
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| 173 | . *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2017**, 36, 351-355 | 2.5 | 7 |
| 172 | Generation of close-to-functional broadside tests with equal primary input vectors **2015**, | | 7 |
| 171 | Reduction of diagnostic fail data volume and tester time using a dynamic N-cover algorithm **2016**, | | 7 |
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| 168 | Static Test Compaction for Scan Circuits by Using Restoration to Modify and Remove Tests. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2014**, 33, 1955-1964 | 2.5 | 7 |
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| 164 | Input Test Data Volume Reduction for Skewed-Load Tests by Additional Shifting of Scan-In States. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2014**, 33, 638-642 | 2.5 | 6 |
| 163 | Signal-Transition Patterns of Functional Broadside Tests. *IEEE Transactions on Computers*, **2013**, 62, 2544-2549 | 2.5 | 6 |
| 162 | Generation of Functional Broadside Tests for Logic Blocks With Constrained Primary Input Sequences. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2013**, 32, 442-452 | 2.5 | 6 |
| 161 | Forming multi-cycle tests for delay faults by concatenating broadside tests **2010**, | | 6 |
| 160 | TOV: Sequential Test Generation by Ordering of Test Vectors. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2010**, 29, 454-465 | 2.5 | 6 |
| 159 | Generation of Mixed Test Sets for Transition Faults. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2012**, 20, 1895-1899 | 2.6 | 6 |
| 158 | Equivalence and Dominance Relations Between Fault Pairs and Their Use in Fault Pair Collapsing for Fault Diagnosis **2007**, | | 6 |
| 157 | Skewed-Load Test Cubes Based on Functional Broadside Tests for a Low-Power Test Set. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2015**, 23, 593-597 | 2.6 | 5 |
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| 155 | On the use of multi-cycle tests for storage of two-cycle broadside tests **2014**, | | 5 |
| 154 | Restoration-Based Procedures With Set Covering Heuristics for Static Test Compaction of Functional Test Sequences. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2014**, 22, 779-791 | 2.6 | 5 |
| 153 | Built-In Generation of Functional Broadside Tests Using a Fixed Hardware Structure. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2013**, 21, 124-132 | 2.6 | 5 |
| 152 | Scan Shift Power of Functional Broadside Tests. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2011**, 30, 1416-1420 | 2.5 | 5 |
| 151 | On Clustering of Undetectable Single Stuck-At Faults and Test Quality in Full-Scan Circuits. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2010**, 29, 1135-1140 | 2.5 | 5 |
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| 148 | Improving the Transition Fault Coverage of Functional Broadside Tests by Observation Point Insertion. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2008**, 16, 931-936 | 2.6 | 5 |
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| 146 | LFSR-Based Test Generation for Path Delay Faults. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2019**, 38, 345-353 | 2.5 | 5 |
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| 144 | $LFSR$ -Based Generation of Partially-Functional Broadside Tests. *IEEE Transactions on Computers*, **2016**, 65, 2659-2664 | 2.5 | 4 |
| 143 | Fault simulation with test switching for static test compaction **2014**, | | 4 |
| 142 | On the detection of path delay faults by functional broadside tests **2012**, | | 4 |
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| 136 | Maximal Independent Fault Set for Gate-Exhaustive Faults. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2021**, 40, 598-602 | 2.5 | 4 |
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| 134 | Test Modification for Reduced Volumes of Fail Data. *ACM Transactions on Design Automation of Electronic Systems*, **2017**, 22, 1-17 | 1.5 | 3 |
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| 131 | An Adjacent Switching Activity Metric under Functional Broadside Tests. *IEEE Transactions on Computers*, **2013**, 62, 404-410 | 2.5 | 3 |
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| 129 | Reducing the Storage Requirements of a Test Sequence by Using One or Two Background Vectors. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2011**, 19, 1755-1764 | 2.6 | 3 |
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| 127 | Hyper-graph based partitioning to reduce DFT cost for pre-bond 3D-IC testing **2011**, | | 3 |
| 126 | Double-Single Stuck-at Faults: A Delay Fault Model for Synchronous Sequential Circuits. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2009**, 28, 426-432 | 2.5 | 3 |
| 125 | Safe Fault Collapsing Based on Dominance Relations **2008**, | | 3 |
| 124 | Diagnostic Test Generation Targeting Equivalence Classes **2007**, | | 3 |
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| 122 | Close-to-Functional Broadside Tests With a Safety Margin. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2017**, 36, 2139-2143 | 2.5 | 2 |
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| 118 | Improving the Accuracy of Defect Diagnosis with Multiple Sets of Candidate Faults. *IEEE Transactions on Computers*, **2016**, 65, 2332-2338 | 2.5 | 2 |
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| 116 | An Initialization Process to Support Online Testing Based on Output Comparison for Identical Finite-State Machines. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2018**, 37, 1494-1504 | 2.5 | 2 |
| 115 | Functional Broadside Test Generation Using a Commercial ATPG Tool **2017**, | | 2 |
| 114 | A bridging fault model for line coverage in the presence of undetected transition faults **2017**, | | 2 |
| 113 | Clock Sequences for Increasing the Fault Coverage of Functional Test Sequences. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2017**, 36, 1231-1235 | 2.5 | 2 |
| 112 | POSTT: Path-oriented static test compaction for transition faults in scan circuits **2017**, | | 2 |
| 111 | Static Test Compaction for Low-Power Test Sets by Increasing the Switching Activity. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2015**, 23, 1936-1940 | 2.6 | 2 |
| 110 | Non-Uniform Coverage by $n$-Detection Test Sets. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2012**, 20, 2138-2142 | 2.6 | 2 |
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| 105 | Broadside and Functional Broadside Tests for Partial-Scan Circuits. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2011**, 19, 1104-1108 | 2.6 | 2 |
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| 102 | Semi-Concurrent On-Line Testing of Transition Faults Through Output Response Comparison of Identical Circuits **2007**, | | 2 |

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| 97 | Input Test Data Volume Reduction Using Seed Complementation and Multiple LFSRs **2020**, | | 2 |
| 96 | On the Switching Activity in Faulty Circuits During Test Application **2016**, | | 2 |
| 95 | Iterative Test Generation for Gate-Exhaustive Faults to Cover the Sites of Undetectable Target Faults **2019**, | | 2 |
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| 92 | Hybrid Pass/Fail and Full Fail Data for Reduced Fail Data Volume. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2021**, 40, 1711-1720 | 2.5 | 2 |
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