Tai-Haur Kuo

List of Publications by Year
in descending order

61 papers	852 citations	567281 15 h-index	526287 27 g-index
61 all docs	61 docs citations	61 times ranked	538 citing authors

#	Article	IF	Citations
1	A 12-bit 40 nm DAC Achieving SFDR > 70 dB at 1.6 GS/s and IMD < –61dB at 2.8 GS/s With DEMDRZ Technique. IEEE Journal of Solid-State Circuits, 2014, 49, 708-717.	5.4	77
2	A wideband CMOS sigma-delta modulator with incremental data weighted averaging. IEEE Journal of Solid-State Circuits, 2002, 37, 11-17.	5.4	73
3	A Compact Dynamic-Performance-Improved Current-Steering DAC With Random Rotation-Based Binary-Weighted Selection. IEEE Journal of Solid-State Circuits, 2012, 47, 444-453.	5.4	72
4	Automatic coefficients design for high-order sigma-delta modulators. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 1999, 46, 6-15.	2.2	66
5	A Current-Mode DCâ€“DC Buck Converter with Efficiency-Optimized Frequency Control and Reconfigurable Compensation. IEEE Transactions on Power Electronics, 2012, 27, 869-880.	7.9	49
6	Low-Cost 14-Bit Current-Steering DAC With a Randomized Thermometer-Coding Method. IEEE Transactions on Circuits and Systems II: Express Briefs, 2009, 56, 137-141.	3.0	47
7	An improved technique for reducing baseband tones in sigma-delta modulators employing data weighted averaging algorithm without adding dither. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 1999, 46, 63-68.	2.2	43
8	Nyquist-Rate Current-Steering Digital-to-Analog Converters With Random Multiple Data-Weighted Averaging Technique and <formula formulatype="inline"><tex>Q^{N}</tex></formula> Rotated Walk Switching Scheme. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2006, 53, 1264-1268.	2.2	42
9	A Single-Inductor Dual-Path Three-Switch Converter With Energy-Recycling Technique for Light Energy Harvesting. IEEE Journal of Solid-State Circuits, 2016, 51, 2716-2728.	5.4	33
10	A Monolithic Capacitor-Current-Controlled Hysteretic Buck Converter With Transient-Optimized Feedback Circuit. IEEE Journal of Solid-State Circuits, 2015, 50, 2524-2532.	5.4	26
11	Advancing Data Weighted Averaging Technique for Multi-Bit Sigma–Delta Modulators. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2007, 54, 838-842.	2.2	25
12	A Four-Phase Buck Converter With Capacitor-Current-Sensor Calibration for Load-Transient-Response Optimization That Reduces Undershoot/Overshoot and Shortens Settling Time to Near Their Theoretical Limits. IEEE Journal of Solid-State Circuits, 2018, 53, 552-568.	5.4	24
13	A 100 W 5.1-Channel Digital Class-D Audio Amplifier With Single-Chip Design. IEEE Journal of Solid-State Circuits, 2012, 47, 1344-1354.	5.4	23
14	16.4 A Calibration-Free 71.7dB SNDR 100MS/s 0.7mW Weighted-Averaging Correlated Level Shifting Pipelined SAR ADC with Speed-Enhancement Scheme. , 2020, , .		23
15	A 75.3-dB SNDR 24-MS/s Ring Amplifier-Based Pipelined ADC Using Averaging Correlated Level Shifting and Reference Swapping for Reducing Errors From Finite Opamp Gain and Capacitor Mismatch. IEEE Journal of Solid-State Circuits, 2019, 54, 1425-1435.	5.4	21
16	A Reconfigurable and Extendable Single-Inductor Single-Path Three-Switch Converter for Indoor Photovoltaic Energy Harvesting. IEEE Journal of Solid-State Circuits, 2020, 55, 1998-2008.	5.4	16
17	A 0.07-mm² 162-mW DAC Achieving >65 dBc SFDR and < â^'70 dBc IM3 at 10 GS/s With Output Impedance Compensation and Concentric Parallelogram Routing. IEEE Journal of Solid-State Circuits, 2020, 55, 2478-2488.	5.4	16
18	A 12-Bit Time-Interleaved 400-MS/s Pipelined ADC With Split-ADC Digital Background Calibration in 4,000 Conversions/Channel. IEEE Transactions on Circuits and Systems II: Express Briefs, 2019, 66, 1810-1814.	3.0	15

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19	Bias-and-Input Interchanging Technique for Cyclic/Pipelined ADCs With Opamp Sharing. IEEE Transactions on Circuits and Systems II: Express Briefs, 2010, 57, 168-172.	3.0	13
20	A Reconfigurable Transient Optimizer Applied to a Four-Phase Buck Converter for Optimizing Both DVS and Load Transient Responses. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 52-56.	3.0	13
21	Current-Mode Converters with Adjustable-Slope Compensating Ramp. , 2006, , .		11
22	A Low Quiescent Current, Low THD+N Class-D Audio Amplifier With Area-Efficient PWM-Residual-Aliasing Reduction. IEEE Journal of Solid-State Circuits, 2018, 53, 3377-3385.	5.4	11
23	A Calibration-Free 14-b 0.7-mW 100-MS/s Pipelined-SAR ADC Using a Weighted- Averaging Correlated Level Shifting Technique. IEEE Journal of Solid-State Circuits, 2020, 55, 3271-3280.	5.4	11
24	Capacitor-Swapping Cyclic A/D Conversion Techniques With Reduced Mismatch Sensitivity. IEEE Transactions on Circuits and Systems II: Express Briefs, 2008, 55, 1219-1223.	3.0	10
25	An automatic coefficient design methodology for high-order bandpass sigma-delta modulator with single-stage structure. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2006, 53, 580-584.	2.2	9
26	A 2.4 mA Quiescent Current, 1 W Output Power Class-D Audio Amplifier With Feed-Forward PWM-Intermodulated-Distortion Reduction. IEEE Journal of Solid-State Circuits, 2016, 51, 1436-1445.	5.4	8
27	A 10-GS/s NRZ/Mixing DAC With Switching-Glitch Compensation Achieving SFDR >64/50 dBc Over the First/Second Nyquist Zone. IEEE Journal of Solid-State Circuits, 2021, 56, 3145-3156.	5.4	8
28	The design of high-order bandpass sigma-delta modulators using low-spread single-stage structure. IEEE Transactions on Circuits and Systems II: Express Briefs, 2004, 51, 202-208.	3.0	7
29	Transfer function design of stable high-order sigma-delta modulators with root locus inside unit circle. , 0, , .		6
30	Transient Output-Current Regulator With Background Calibration Applied to a Buck Converter for Fast Load-Transient Response. IEEE Solid-State Circuits Letters, 2020, 3, 462-465.	2.0	5
31	A 3 mW 6-bit 4 GS/s Subranging ADC With Subrange-Dependent Embedded References. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 2312-2316.	3.0	5
32	A 0.82mW 14b 130MS/S Pipelined-SAR ADC With a Distributed Averaging Correlated Level Shifting (DACLS) Ringamp and Bypass-Window Backend. , 2022, , .		5
33	A 4.86 mW 15-bit 22.5 MS/s pipelined ADC with 74 dB SNDR in 90 nm CMOS using averaging correlated level shifting technique. , 2016, , .		4
34	27.6 Background Capacitor-Current-Sensor Calibration of DC-DC Buck Converter with DVS for Accurately Accelerating Load-Transient Response. , 2019, , .		4
35	Optimal Design for Deltaâ€“Sigma Modulators With Root Loci Inside Unit Circle. IEEE Transactions on Circuits and Systems II: Express Briefs, 2012, 59, 83-87.	3.0	3
36	A monolithic capacitor-current-controlled hysteretic buck converter with transient-optimized feedback circuit. , 2014, , .		3

#	Article	IF	Citations
37	A 3mW 6b 4GS/s Subranging ADC with Adaptive Offset-Adjustable Comparators. , 2019, , .		3
38	Development of intellectual property for Brushless DC Motor drives. , 2011, , .		2
39	A low-spurious low-power 12-bit 300MS/s DAC with 0.1mm² in 0.18µm CMOS process. , 2013, , .		2
40	A Light Energy Harvesting Single-Inductor Dual-Input Dual-Output Converter for WSN. , 2019, , .		2
41	An Analog Optimum Torque Control IC for a 200-W Wind Energy Harvesting System. IEEE Transactions on Circuits and Systems II: Express Briefs, 2019, 66, 1790-1794.	3.0	2
42	23.5 A 0.41mA Quiescent Current, 0.00091% THD+N Class-D Audio Amplifier with Frequency Equalization for PWM-Residual-Aliasing Reduction. , 2020, , .		2
43	Fixed-Switching-Frequency Background Capacitor-Current-Sensor Calibration for DCâ€“DC Converters. IEEE Journal of Solid-State Circuits, 2022, 57, 1504-1516.	5.4	2
44	A 0.4-mA-Quiescent-Current, 0.00091%-THD+N Class-D Audio Amplifier With Low-Complexity Frequency Equalization for PWM-Residual- Aliasing Reduction. IEEE Journal of Solid-State Circuits, 2022, 57, 423-433.	5.4	2
45	Design and analysis of fourth-order leapfrog topologies for sigma-delta A/D converters. , 0, , .		1
46	Offset current cancellation based on a multiple-path feedback compensation (MPFC) technique for switched-current circuits and systems. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 1997, 44, 299-309.	2.2	1
47	High-speed DACs with random multiple data-weighted averaging algorithm. , 0, , .		1
48	Optimizing the efficiency of DC-DC converters with an analog variable-frequency controller. , 2008, , .		1
49	A 12-bit cyclic ADC with random feedback capacitor interchanging technique. , 2009, , .		1
50	Leading-Subcycles Capacitor Error-Averaging Scheme for Cyclic ADCs. IEEE Transactions on Instrumentation and Measurement, 2011, 60, 776-783.	4.7	1
51	Slew-rate controlled output stages for switching DC-DC converters. , 2011, , .		1
52	A compact low-power flash ADC using auto-zeroing with capacitor averaging. , 2013, , .		1
53	Modeling and simulation of vertically integrated resonant tunneling diode based high-speed circuits. Optical Engineering, 1993, 32, 131.	1.0	0
54	High-speed low-complexity implementation for data weighted averaging algorithm [Î£Î” modulator applications]. , 0, , .		0

#	Article	IF	Citations
55	Random Incrementing Data Weighted Averaging for Nyquist-rate Digital-to-Analog Converters. , 2007, , .		0
56	A Cyclic A/D Conversion Technique with Improved SFDR. , 2007, , .		0
57	A load-transient-enhanced wireless power transfer system via transmitter-side regulator. , 2014, , .		0
58	Introduction to the Special Issue on the 2018 IEEE International Solid-State Circuits Conference (ISSCC). IEEE Journal of Solid-State Circuits, 2018, 53, 3343-3346.	5.4	0
59	A 40/30 MS/s Dual-Mode Pipelined ADC with Error Averaging Techniques in 90nm CMOS Achieving 71.2/74.5 dB SNDR over the Entire Nyquist Bandwidth. , 2019, , .		0
60	A 0.07mm² 210mW Single-1.1V-Supply 14-bit 10GS/s DAC with Concentric Parallelogram Routing and Output Impedance Compensation. , 2019, , .		0
61	A 15-bit 20 MS/s SHA-Less Pipelined ADC Achieving 73.7 dB SNDR with Averaging Correlated Level Shifting Technique. , 2019, , .		0