Eduardo QuiÃ±ones

List of Publications by Year
in descending order

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64 papers	1,671 citations	933447 10 h-index	794594 19 g-index
67 all docs	67 docs citations	67 times ranked	479 citing authors

#	Article	IF	Citations
1	The OpenMP API for High Integrity Systems. ACM SIGAda Ada Letters, 2021, 40, 48-50.	0.1	2
2	Real-time Issues in the Ada Parallel Model with OpenMP. ACM SIGAda Ada Letters, 2021, 40, 96-102.	0.1	0
3	Enabling Ada and OpenMP runtimes interoperability through template-based execution. Journal of Systems Architecture, 2020, 105, 101702.	4.3	2
4	Combining the tasklet model with OpenMP. ACM SIGAda Ada Letters, 2018, 38, 14-18.	0.1	1
5	Adapting TDMA arbitration for measurement-based probabilistic timing analysis. Microprocessors and Microsystems, 2017, 52, 188-201.	2.8	1
6	Fitting processor architectures for measurement-based probabilistic timing analysis. Microprocessors and Microsystems, 2016, 47, 287-302.	2.8	29
7	PROXIMA: Improving Measurement-Based Timing Analysis through Randomisation and Probabilistic Analysis. , 2016, , .		20
8	pTNoC: Probabilistically Time-Analyzable Tree-Based NoC for Mixed-Criticality Systems. , 2016, , .		5
9	TASA. , 2016, , .		11
10	Parallelizing Industrial Hard Real-Time Applications for the parMERASA Multicore. Transactions on Embedded Computing Systems, 2016, 15, 1-27.	2.9	14
11	Timing Analysis of an Avionics Case Study on Complex Hardware/Software Platforms. , 2015, , .		24
12	OpenMP and Timing Predictability: A Possible Union?. , 2015, , .		27
13	CAP: Communication-Aware Allocation Algorithm for Real-Time Parallel Applications on Many-Cores. , 2015, , .		1
14	Resource usage templates and signatures for COTS multicore processors. , 2015, , .		8
15	P-SOCRATES: A parallel software framework for time-critical many-core systems. Microprocessors and Microsystems, 2015, 39, 1190-1203.	2.8	11
16	WCET analysis methods: Pitfalls and challenges on their trustworthiness. , 2015, , .		65
17	Introduction to partial time composability for COTS multicores. , 2015, , .		3
18	Increasing confidence on measurement-based contention bounds for real-time round-robin buses. , 2015, , .		12

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19	Parallel execution of AUTOSAR legacy applications on multicore ECUs with timed implicit communication. , 2015, , .		15
20	PACO. , 2015, , .		0
21	Speeding up Static Probabilistic Timing Analysis. Lecture Notes in Computer Science, 2015, , 236-247.	1.3	4
22	A Dual-Criticality Memory Controller (DCmc): Proposal and Evaluation of a Space Case Study. , 2014, , .		36
23	Measurement-Based Probabilistic Timing Analysis and Its Impact on Processor Architecture. , 2014, , .		20
24	RunPar. , 2014, , .		27
25	PUB: Path Upper-Bounding for Measurement-Based Probabilistic Timing Analysis. , 2014, , .		16
26	On the Comparison of Deterministic and Probabilistic WCET Estimation Techniques. , 2014, , .		46
27	Time-Analysable Non-Partitioned Shared Caches for Real-Time Multicore Systems. , 2014, , .		19
28	AHRB: A high-performance time-composable AMBA AHB bus. , 2014, , .		6
29	Timing Verification of Fault-Tolerant Chips for Safety-Critical Applications in Harsh Environments. IEEE Micro, 2014, 34, 8-19.	1.8	10
30	Bus designs for time-probabilistic multicore processors. , 2014, , .		15
31	P-SOCRATES: A Parallel Software Framework for Time-Critical Many-Core Systems. , 2014, , .		5
32	Heart of Gold: Making the Improbable Happen to Increase Confidence in MBPTA. , 2014, , .		23
33	Efficient Cache Designs for Probabilistically Analysable Real-Time Systems. IEEE Transactions on Computers, 2014, 63, 2998-3011.	3.4	12
34	Bus designs for time-probabilistic multicore processors. , 2014, , .		7
35	DTM: Degraded Test Mode for Fault-Aware Probabilistic Timing Analysis. , 2013, , .		20
36	A Cache Design for Probabilistically Analysable Real-time Systems. , 2013, , .		48

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37	Deconstructing bus access control policies for Real-Time multicores. , 2013, , .		20
38	Multi-level Unified Caches for Probabilistically Time Analysable Real-Time Systems. , 2013, , .		21
39	Probabilistic Timing Analysis on Conventional Cache Designs. , 2013, , .		19
40	Timing effects of DDR memory systems in hard real-time multicore architectures. Transactions on Embedded Computing Systems, 2013, 12, 1-26.	2.9	34
41	On the convergence of mainstream and mission-critical markets. , 2013, , .		6
42	A hard real-time capable multi-core SMT processor. Transactions on Embedded Computing Systems, 2013, 12, 1-26.	2.9	16
43	Achieving timing composability with measurement-based probabilistic timing analysis. , 2013, , .		11
44	Measurement-based probabilistic timing analysis: Lessons from an integrated-modular avionics case study. , 2013, , .		50
45	parMERASA -- Multi-core Execution of Parallelised Hard Real-Time Applications Supporting Analysability. , 2013, , .		34
46	PROARTIS. Transactions on Embedded Computing Systems, 2013, 12, 1-26.	2.9	89
47	On the evaluation of the impact of shared resources in multithreaded COTS processors in time-critical environments. Transactions on Architecture and Code Optimization, 2012, 8, 1-25.	2.0	52
48	Assessing the suitability of the NGMP multi-core processor in the space domain. , 2012, , .		40
49	Measurement-Based Probabilistic Timing Analysis for Multi-path Programs. , 2012, , .		159
50	A Software-Pipelined Approach to Multicore Execution of Timing Predictable Multi-threaded Hard Real-Time Tasks. , 2011, , .		7
51	RVC-based time-predictable faulty caches for safety-critical systems. , 2011, , .		9
52	IA^3: An Interference Aware Allocation Algorithm for Multicore Hard Real-Time Systems. , 2011, , .		25
53	Towards improved survivability in safety-critical systems. , 2011, , .		14
54	RVC. , 2011, , .		12

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55	Exploiting intra-task slack time of load operations for DVFS in hard real-time multi-core systems. ACM SIGBED Review, 2011, 8, 32-35.	1.8	5
56	Merasa: Multicore Execution of Hard Real-Time Applications Supporting Analyzability. IEEE Micro, 2010, 30, 66-75.	1.8	119
57	Leveraging Register Windows to Reduce Physical Registers to the Bare Minimum. IEEE Transactions on Computers, 2010, 59, 1598-1610.	3.4	3
58	Hardware support for WCET analysis of hard real-time multicore systems. Computer Architecture News, 2009, 37, 57-68.	2.5	40
59	Using Randomized Caches in Probabilistic Real-Time Systems. , 2009, , .		32
60	An Analyzable Memory Controller for Hard Real-Time CMPs. IEEE Embedded Systems Letters, 2009, 1, 86-90.	1.9	111
61	Hardware support for WCET analysis of hard real-time multicore systems. , 2009, , .		151
62	Improving Branch Prediction and Predicated Execution in Out-of-Order Processors. , 2007, , .		10
63	Early Register Release for Out-of-Order Processors with RegisterWindows. Parallel Architecture and Compilation Techniques (PACT), Proceedings of the International Conference on, 2007, , .	0.0	3
64	Selective predicate prediction for out-of-order processors. , 2006, , .		6