Alper Buyuktosunoglu

List of Publications by Year
in descending order

19	831	1684188 5	1281871 11
papers	citations	h-index	g-index

19	19	19	583
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	AI accelerator on IBM Telum processor. , 2022, , .		3
2	Intelligent Adaptation of Hardware Knobs for Improving Performance and Power Consumption. IEEE Transactions on Computers, 2021, 70, 1-16.	3.4	3
3	Predictive Guardbanding: Program-Driven Timing Margin Reduction for GPUs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 171-184.	2.7	5
4	Cores, Cache, Content, and Characterization: IBMâ€™s Second Generation 14-nm Product, z15. IEEE Journal of Solid-State Circuits, 2021, 56, 98-111.	5.4	4
5	TokenSmart: Distributed, Scalable Power Management in the Many-Core Era. IEEE Computer Architecture Letters, 2021, 20, 42-45.	1.5	0
6	Energy Efficiency Boost in the AI-Infused POWER10 Processor. , 2021, , .		8
7	Heterogeneity-Aware Scheduling on SoCs for Autonomous Vehicles. IEEE Computer Architecture Letters, 2021, 20, 82-85.	1.5	6
8	Asymmetric Resilience: Exploiting Task-Level Idempotency for Transient Error Recovery in Accelerator-Based Systems. , 2020, , .		14
9	Asymmetric Resilience for Accelerator-Rich Systems. IEEE Computer Architecture Letters, 2019, 18, 83-86.	1.5	2
10	IBM z14: Processor Characterization and Power Management for High-Reliability Mainframe Systems. IEEE Journal of Solid-State Circuits, 2019, 54, 121-132.	5.4	11
11	Droop mitigation using critical-path sensors and an on-chip distributed power supply estimation engine in the z14â„¢ enterprise processor. , 2018, , .		16
12	Safe limits on voltage reduction efficiency in GPUs. , 2015, , .		60
13	Voltage Noise in Multi-Core Processors: Empirical Characterization and Optimization Opportunities. , 2014, , .		52
14	Crank it up or dial it down. , 2013, , .		55
15	Introducing the Adaptive Energy Management Features of the Power7 Chip. IEEE Micro, 2011, 31, 60-75.	1.8	95
16	Energy-Aware Accounting and Billing in Large-Scale Computing Facilities. IEEE Micro, 2011, 31, 60-71.	1.8	14
17	Program behavior prediction using a statistical metric model. Performance Evaluation Review, 2010, 38, 371-372.	0.6	2
18	CPU Accounting in CMP Processors. IEEE Computer Architecture Letters, 2009, 8, 17-20.	1.5	9

#	Article	IF	Citations
19	An Analysis of Efficient Multi-Core Global Power Management Policies: Maximizing Performance for a Given Power Budget. Microarchitecture (MICRO), Proceedings of the Annual International Symposium on, 2006, , .	0.0	472