# Yuan Du

List of Publications by Year
in descending order



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|---|---|---|---|
| 23 papers | 334 citations | 1478505 6 h-index | 996975 15 g-index |
| 23 all docs | 23 docs citations | 23 times ranked | 496 citing authors |

| # | Article | IF | Citations |
|---|---|---|---|
| 1 | Memory-Efficient CNN Accelerator Based on Interlayer Feature Map Compression. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 668-681. | 5.4 | 11 |
| 2 | A Low-Power High-Accuracy Urban Waterlogging Depth Sensor Based on Millimeter-Wave FMCW Radar. Sensors, 2022, 22, 1236. | 3.8 | 3 |
| 3 | An Efficient High-Throughput Structured-Light Depth Engine. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2022, 30, 1047-1058. | 3.1 | 2 |
| 4 | A Contactless Glucose Solution Concentration Measurement System Based on Improved High Accurate FMCW Radar Algorithm. Sensors, 2022, 22, 4126. | 3.8 | 0 |
| 5 | Prototype-Voxel Contrastive Learning for LiDAR Point Cloud Panoptic Segmentation. , 2022, , . | | 3 |
| 6 | A DNN Optimization Framework with Unlabeled Data for Efficient and Accurate Reconfigurable Hardware Inference. , 2021, , . | | 2 |
| 7 | Characterization of Programmable Charge-Trap Transistors (CTTs) in Standard 28-nm CMOS for Nonvolatile Memory and Analog Arithmetic Applications. IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, 2021, 7, 10-17. | 1.5 | 5 |
| 8 | Flexible-width Bit-level Compressor for Convolutional Neural Network. , 2021, , . | | 2 |
| 9 | CTT-based Non-Volatile Deep Neural Network Accelerator Design. , 2021, , . | | 1 |
| 10 | A Reconfigurable 64-Dimension K-Means Clustering Accelerator With Adaptive Overflow Control. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 760-764. | 3.0 | 3 |
| 11 | In-Memory Computing: The Next-Generation AI Computing Paradigm. , 2020, , . | | 9 |
| 12 | A Reconfigurable Permutation Based Address Encryption Architecture for Memory Security. , 2020, , . | | 0 |
| 13 | An Analog Neural Network Computing Engine Using CMOS-Compatible Charge-Trap-Transistor (CTT). IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 1811-1819. | 2.7 | 28 |
| 14 | A Millimeter-Wave CMOS Transceiver With Digitally Pre-Distorted PAM-4 Modulation for Contactless Communications. IEEE Journal of Solid-State Circuits, 2019, 54, 1600-1612. | 5.4 | 19 |
| 15 | A 7.5-mW 10-Gb/s 16-QAM wireline transceiver with carrier synchronization and threshold calibration for mobile inter-chip communications in 16-nm FinFET. , 2019, , . | | 0 |
| 16 | A Reconfigurable Streaming Deep Convolutional Neural Network Accelerator for Internet of Things. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 198-208. | 5.4 | 153 |
| 17 | A 2-GS/s 8-Bit ADC Featuring Virtual-Ground Sampling Interleaved Architecture in 28-nm CMOS. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 1534-1538. | 3.0 | 6 |
| 18 | A Single Layer 3-D Touch Sensing System for Mobile Devices Application. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 286-296. | 2.7 | 7 |

| # | Article | IF | Citations |
|---|---|---|---|
| 19 | A 32-Gb/s C2C-DAC-Based PAM-4 Wireline Transmitter With Two-Tap Feed-Forward Equalization and Level-Mismatch Correction in 28-nm CMOS. IEEE Microwave and Wireless Components Letters, 2018, 28, 1056-1058. | 3.2 | 2 |
| 20 | A 16-Gb/s 14.7-mW Tri-Band Cognitive Serial Link Transmitter With Forwarded Clock to Enable PAM-16/256-QAM and Channel Response Detection. IEEE Journal of Solid-State Circuits, 2017, 52, 1111-1122. | 5.4 | 24 |
| 21 | Impulse response analysis of carrier-modulated multiband RF-interconnect (MRFI). Analog Integrated Circuits and Signal Processing, 2017, 93, 395-413. | 1.4 | 2 |
| 22 | An R2R-DAC-Based Architecture for Equalization-Equipped Voltage-Mode PAM-4 Wireline Transmitter Design. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 3260-3264. | 3.1 | 4 |
| 23 | A 0.56 THz Phase-Locked Frequency Synthesizer in 65 nm CMOS Technology. IEEE Journal of Solid-State Circuits, 2016, 51, 3005-3019. | 5.4 | 48 |