Lei He

List of Publications by Year in Descending Order

93 papers	1,143 citations	15 h-index	30 g-index
113 ext. papers	1,431 ext. citations	2.9 avg, IF	4.39 L-index

#	Paper	IF	Citations
93	Low-precision Floating-point Arithmetic for High-performance FPGA-based CNN Acceleration. *ACM Transactions on Reconfigurable Technology and Systems*, **2022**, 15, 1-21	2.7	3
92	MP-OPU: A Mixed Precision FPGA-based Overlay Processor for Convolutional Neural Networks **2021**,		2
91	Exploring Instance-Level Uncertainty for Medical Detection **2021**,		1
90	Channel-Correlation-Enabled Transmission Optimization for MISO Wiretap Channels. *IEEE Transactions on Wireless Communications*, **2021**, 20, 858-870	9.6	11
89	Effective Scaling of Blockchain Beyond Consensus Innovations and Moore's Law: Challenges and Opportunities. *IEEE Systems Journal*, **2021**, 1-12	4.3	0
88	. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2020**, 28, 1545-1556	2.6	5
87	QoS-Based Robust Cooperative-Jamming-Aided Beamforming for Correlated Wiretap Channels. *IEEE Signal Processing Letters*, **2020**, 27, 216-220	3.2	4
86	. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2020**, 39, 4999-5010	2.5	2
85	Robust Beamforming Design for Correlated MISO Wiretap Channels Under Channel Uncertainty. *IEEE Wireless Communications Letters*, **2020**, 9, 553-557	5.9	1
84	Correlation-Based Cooperative Jamming to Enhance Secrecy With Receiver-Side Correlation. *IEEE Transactions on Vehicular Technology*, **2020**, 69, 1903-1912	6.8	3
83	Correlation-Based Secure Transmission for Correlated MISO Wiretap Channels. *IEEE Wireless Communications Letters*, **2020**, 9, 302-305	5.9	3
82	OPU: An FPGA-Based Overlay Processor for Convolutional Neural Networks. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2020**, 28, 35-47	2.6	27
81	Multiple-Jammer-Aided Secure Transmission With Receiver-Side Correlation. *IEEE Transactions on Wireless Communications*, **2019**, 18, 3093-3103	9.6	12
80	AN-Aided Secure Beamforming Design for Correlated MISO Wiretap Channels. *IEEE Communications Letters*, **2019**, 23, 628-631	3.8	6
79	IEEE Access Special Section Editorial: The Internet of Energy: Architectures, Cyber Security, and Applications. *IEEE Access*, **2018**, 6, 79272-79275	3.5	3
78	IEEE Access Special Section Editorial: The Internet of Energy: Architectures, Cyber Security, and Applications—Part II. *IEEE Access*, **2018**, 6, 79276-79279	3.5	3
77	Modeling and Implementation of Electroactive Smart Air-Conditioning Vent Register for Personalized HVAC Systems. *IEEE Access*, **2017**, 5, 1649-1657	3.5	3

76	Grain Price Forecasting Using a Hybrid Stochastic Method. *Asia-Pacific Journal of Operational Research*, **2017**, 34, 1750020	0.8	2
75	Layout driven FPGA packing algorithm for performance optimization. *IEICE Electronics Express*, **2017**, 14, 20170419-20170419	0.5	
74	Sampling and Reconstruction in Arbitrary Measurement and Approximation Spaces Associated With Linear Canonical Transform. *IEEE Transactions on Signal Processing*, **2016**, 64, 6379-6391	4.8	43
73	Incremental Latin hypercube sampling for lifetime stochastic behavioral modeling of analog circuits **2015**,		2
72	A fast and provably bounded failure analysis of memory circuits in high dimensions **2014**,		13
71	IPF: In-Place X-Filling Algorithm for the Reliability of Modern FPGAs. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2014**, 22, 2226-2229	2.6	5
70	Accelerating the iterative linear solver for reservoir simulation on multicore architectures **2014**,		1
69	A parallel attractor-finding algorithm based on Boolean satisfiability for genetic regulatory networks. *PLoS ONE*, **2014**, 9, e94258	3.7	21
68	Stochastic Behavioral Modeling and Analysis for Analog/Mixed-Signal Circuits. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2013**, 32, 24-33	2.5	13
67	Fast Filter-Based Boolean Matchers. *IEEE Embedded Systems Letters*, **2013**, 5, 65-68	1	1
66	Stochastic behavioral modeling of analog/mixed-signal circuits by maximizing entropy **2013**,		6
65	Modeling and Application of Multi-Port TSV Networks in 3-D IC. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2013**, 32, 487-496	2.5	34
64	eCushion: A Textile Pressure Sensor Array Design and Calibration for Sitting Posture Analysis. *IEEE Sensors Journal*, **2013**, 13, 3926-3934	4	107
63	A Parallel and Incremental Extraction of Variational Capacitance With Stochastic Geometric Moments. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2012**, 20, 1729-1737	2.6	4
62	Heterogeneous configuration memory scrubbing for soft error mitigation in FPGAs **2012**,		10
61	Fourier Series Approximation for Max Operation in Non-Gaussian and Quadratic Statistical Static Timing Analysis. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2012**, 20, 1383-1391	2.6	8
60	Worst-Case Estimation for Data-Dependent Timing Jitter and Amplitude Noise in High-Speed Differential Link. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2012**, 20, 89-97	2.6	1
59	In-Place FPGA Retiming for Mitigation of Variational Single-Event Transient Faults. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2011**, 58, 1372-1381	3.9	8

58	Runtime Resonance Noise Reduction with Current Prediction Enabled Frequency Actuator. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2011**, 19, 508-512	2.6	2
57	Physically Justifiable Die-Level Modeling of Spatial Variation in View of Systematic Across Wafer Variability. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2011**, 30, 388-401	2.5	21
56	Mitigating FPGA interconnect soft errors by in-place LUT inversion **2011**,		7
55	IPF: In-Place X-Filling to Mitigate Soft Errors in SRAM-Based FPGAs **2011**,		5
54	Acceleration of Multi-agent Simulation on FPGAs **2011**,		3
53	Fast Analysis of a Large-Scale Inductive Interconnect by Block-Structure-Preserved Macromodeling. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2010**, 18, 1399-1411	2.6	8
52	RALF: Reliability Analysis for Logic Faults An exact algorithm and its applications **2010**,		4
51	Engineering a scalable Boolean matching based on EDA SaaS 2.0 **2010**,		1
50	Fault-tolerant resynthesis with dual-output LUTs **2010**,		9
49	Modeling and design for beyond-the-die power integrity **2010**,		3
48	In-place decomposition for robustness in FPGA **2010**,		10
47	Optimality and Improvement of Dynamic Voltage Scaling Algorithms for Multimedia Applications. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2010**, 57, 681-690	3.9	19
46	EMPIRE: An Efficient and Compact Multiple-Parameterized Model-Order Reduction Method for Physical Optimization. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2010**, 18, 108-118	2.6	0
45	Technology Mapping and Clustering for FPGA Architectures With Dual Supply Voltages. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2010**, 29, 1709-1722	2.5	6
44	Accelerating Boolean Matching Using Bloom Filter. *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, **2010**, E93-A, 1775-1781	0.4	3
43	Dynamic power and thermal integrity in 3D integration **2009**,		2
42	Accounting for non-linear dependence using function driven component analysis **2009**,		4
41	Worst case timing jitter and amplitude noise in differential signaling **2009**,		1

40	Design and Synthesis of Programmable Logic Block With Mixed LUT and Macrogate. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2009**, 28, 591-595	2.5	4
39	Efficient Decoupling Capacitance Budgeting Considering Operation and Process Variations. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2008**, 27, 1253-1263	2.5	15
38	Dual-V_{dd} Buffer Insertion for Power Reduction. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2008**, 27, 1498-1502	2.5	1
37	Robust FPGA resynthesis based on fault-tolerant Boolean matching **2008**,		4
36	Scalable Symbolic Model Order Reduction **2008**,		3
35	Stochastic Physical Synthesis Considering Prerouting Interconnect Uncertainty and Process Variation for FPGAs. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2008**, 16, 124-133	2.6	11
34	Simultaneous buffer insertion and wire sizing considering systematic CMP variation and random leff variation. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2007**, 26, 845-857	2.5	
33	Efficient decoupling capacitance budgeting considering operation and process variations. *IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers*, **2007**,		1
32	DpRouter: A Fast and Accurate Dynamic-Pattern-Based Global Routing Algorithm **2007**,		19
31	Design, synthesis and evaluation of heterogeneous FPGA with mixed LUTs and macro-gates. *IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers*, **2007**,		2
30	Robust Extraction of Spatial Correlation. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2007**, 26, 619-631	2.5	112
29	Field Programmability of Supply Voltages for FPGA Power Reduction. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2007**, 26, 752-764	2.5	15
28	Efficient In-Package Decoupling Capacitor Optimization for I/O Power Integrity. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2007**, 26, 734-738	2.5	25
27	Device and Architecture Cooptimization for FPGA Power Reduction. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2007**, 26, 1211-1221	2.5	8
26	TermMerg: An Efficient Terminal-Reduction Method for Interconnect Circuits. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2007**, 26, 1382-1392	2.5	8
25	Device and architecture concurrent optimization for FPGA transient soft error rate. *IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers*, **2007**,		5
24	Exploiting symmetry in SAT-based boolean matching for heterogeneous FPGA technology mapping. *IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers*, **2007**,		5
23	Microarchitecture Configurations and Floorplanning Co-Optimization. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2007**, 15, 830-841	2.6	2

22	Placement and Timing for FPGAs Considering Variations **2006**,		16
21	Circuit simulation based obstacle-aware Steiner routing. *Proceedings - Design Automation Conference*, **2006**,		3
20	Wideband passive multiport model order reduction and realization of RLCM circuits. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2006**, 25, 1496-1509	2.5	15
19	Modeling and synthesis of multiport transmission line for multichannel communication. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2006**, 25, 1664-1676	2.5	1
18	Piecewise linear model for transmission line with capacitive loading and ramp input. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2005**, 24, 928-937	2.5	10
17	A provably passive and cost-efficient model for inductive interconnects. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2005**, 24, 1283-1294	2.5	5
16	Worst case crosstalk noise for nonswitching victims in high-speed buses. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2005**, 24, 1275-1283	2.5	5
15	Temperature and supply Voltage aware performance and power modeling at microarchitecture level. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2005**, 24, 1042-1053	2.5	172
14	Power modeling and characteristics of field programmable gate arrays. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2005**, 24, 1712-1724	2.5	64
13	Extended global routing with RLC crosstalk constraints. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2005**, 13, 319-329	2.6	5
12	Microarchitecture-level leakage reduction with data retention. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2005**, 13, 1324-1328	2.6	7
11	Distributed sleep transistor network for power reduction. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2004**, 12, 937-946	2.6	65
10	Full-chip routing optimization with RLC crosstalk budgeting. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2004**, 23, 366-377	2.5	8
9	Full-chip interconnect power estimation and simulation considering concurrent repeater and flip-flop insertion **2003**,		3
8	An efficient method for terminal reduction of interconnect circuits considering delay variations		6
7	A sparsified vector potential equivalent circuit model for massively coupled interconnects		1
6	Block structure preserving model order reduction		6
5	Vdd programmability to reduce FPGA interconnect power		16

List of Publications

4	Wideband modeling of RF/analog circuits via hierarchical multi-point model order reduction	3
3	A wideband hierarchical circuit reduction for massively coupled interconnects	1
2	Routing track duplication with fine-grained power-gating for FPGA interconnect power reduction	5
1	Staggered twisted-bundle interconnect for crosstalk and delay reduction	3